S NO	IEEE	TITLE
1	2017	Efficient Hardware Implementation of Probabilistic Gradient Descent Bit-Flipping
2	2017	Reliability Enhancement of Low-power sequential circuits using reconfigurable Pulsed Latches
3	2017	Design for testability of sleep convention logic
4	2017	LFSR-Based Generation of Multi cycle Tests
5	2017	Scalable Approach for Power Droop Reduction During Scan-Based Logic BIST
6	2017	Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test Pattern Generation and Reseeding
7	2017	A Bit plane Decomposition Matrix Based VLSI Integer Transform Architecture for HEVC
8	2017	Low Complexity and Critical Path based VLSI Architecture for LMS Adaptive Filter using Distributed Arithmetic
9	2017	Probabilistic Error Modeling for Approximate Adders
10	2017	Fault Space Transformation: A Generic Approach to Counter Differential Fault Analysis and Differential Fault Intensity Analysis on AES-like Block Ciphers
11	2017	Weighted Partitioning for Fast Multiplierless Multiple-Constant Convolution Circuit
12	2017	Efficient RNS Scalers for the Extended Three-Moduli Set (2n -1; 2n+p; 2n + 1)
13	2017	Reconfigurable Constant Multiplication for FPGAs
14	2017	DLAU: A Scalable Deep Learning Accelerator Uniton FPGA
15	2017	Optimization of Constant Matrix Multiplication with Low Power and High Throughput
16	2017	An Optimized 3x3 Shift and Add Multiplier on FPGA
17	2017	Low Latency and Low Error Floating-Point Sine/Cosine Function Based TCORDIC Algorithm
18	2017	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing
19	2017	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder
20	2017	Probabilistic Error Analysis of Approximate Recursive Multipliers
21	2017	Optimal Design of Reversible Parity Preserving New Full Adder / Full Subtractor
22	2017	On the Implementation of Computation-in-Memory Parallel Adder
23	2017	Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction
24	2017	High-Speed and Low-Power VLSI-Architecture for Inexact Speculative Adder
25	2017	High Performance Parallel Decimal Multipliers using Hybrid BCD Codes
26	2017	Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression
27	2017	Design and Analysis of Multiplier Using Approximate 15-4 Compressor
28	2017	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication
29	2017	Majority-Logic-Optimized Parallel Prefix Carry Look-Ahead Adder Families Using Adiabatic Quantum-Flux-Parametron Logic
30	2017	Energy-Efficient VLSI Realization of Binary64 Division With Redundant Number Systems

31	2017	DSP48E Efficient Floating Point Multiplier Architectures on FPGA
32	2017	Fast Energy Efficient Radix-16 Sequential Multiplier
33	2017	A Residue-to-Binary Converter for the Extended Four-Moduli Set {2nâˆ’ 1, 2n+ 1, 22n+ 1, 22n+p}
34	2017	Majority Logic Formulations for Parallel Adder Designs at Reduced Delay and Circuit Complexity
35	2017	Design And Synthesis Of Combinational Circuits Using Reversible Decoder In Xilinx
36	2017	Design of Approximate Radix-4 Booth Multipliers for Error-Tolerant Computing
37	2017	Design of Power and Area Efficient Approximate Multipliers
38	2017	Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers
39	2017	A Slack-based Approach to Efficiently Deploy Radix 8 Booth Multipliers
40	2017	A Low Error Energy-Efficient Fixed-Width Booth Multiplier with Sign-Digit-Based Conditional Probability Estimation
41	2016	Design of high speed multiplier using Modified Booth Algorithm with hybrid carry look-ahead adder
42	2016	An Improved Design of a Reversible Fault Tolerant LUT-Based FPGA
43	2016	Energy-Aware Scheduling of FIR Filter Structures using a Timed Automata Model
44	2016	Design Of High Speed Multiplier Using Modified Booth Algorithm With Hybrid Carry Look-Ahead Adder
45	2016	Design Of Low Power, High Performance 2-4 And 4-16 Mixed-Logic Line Decoders
46	2016	High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels
47	2016	Design of Register File using Reversible Logic
48	2016	Low-Quantum Cost Circuit Constructions for Adder and Symmetric Boolean Functions
49	2016	Squaring in Reversible Logic using Zero Garbage and Reduced Ancillary inputs
50	2016	Improved Synthesis of Reversible Sequential Circuits
51	2016	A Low-Power Robust Easily Cascaded Pentamtj-Based Combinational And Sequential Circuits
52	2016	Low-Power Ask Detector For Low Modulation Indexes And Rail-To-Rail Input Range
53	2016	A Low-Power Incremental Deltaâ€“Sigma Adc For Cmos Image Sensors
54	2016	A 55-Ghz-Bandwidth Track-And-Hold Amplifier In 28-Nm Low-Power Cmos
55	2016	A Low Power Trainable Neuromorphic Integrated Circuit That Is Tolerant To Device Mismatch
56	2016	Pns-Fcr: Flexible Charge Recycling Dynamic Circuit Technique For Low-Power Microprocessors
57	2016	Low-Power Variation-Tolerant Nonvolatile Lookup Table Design
58	2016	Dual Use Of Power Lines For Design-For-Testabilityâ€”A Cmos Receiver Design
59	2016	A 28 nm Configurable Memory (TCAM/BCAM/SRAM) Using Push-Rule 6T Bit Cell Enabling Logic-in-Memory
60	2016	Arithmetic algorithms for extended precision using floating-point expansions
61	2016	Hybrid Lut/Multiplexer Fpga Logic Architectures
62	2016	Hardware And Energy-Efficient Stochastic Lu Decomposition Scheme For Mimo Receivers
63	2016	Input-Based Dynamic Reconfiguration Of Approximate Arithmetic Units For Video Encoding

64	2016	High-Speedand Energy-Efficient Carry Skip Adder Operating Under A Wide Rangeof Supply Voltage Levels
65	2016	VLSI Design for Convolutive Blind Source Separation
66	2016	A High-Speed FPGA Implementation of an RSD-Based ECC Processor
67	2016	Low-Cost High-Performance Vlsi Architecture For Montgomery Modular Multiplication
68	2016	High Speed Hybrid Double Multiplication Architectures Using New Serial-Out Bit- Level Mastrovito Multipliers
69	2016	A Normal I/O Order Radix-2 Fft Architecture To Process Twin Data Streams For Mimo
70	2016	A Cellular Network Architecture With Polynomial Weight Functions
71	2016	A Modified Partial Product Generator For Redundant Binary Multipliers
72	2016	A High Throughput List Decoder Architecture for Polar Codes
73	2016	A Novel Coding Scheme For Secure Communications In Distributed Rfid Systems
74	2016	Design for Testability of Sleep Convention Logic
75	2016	Memory-Reduced Turbo Decoding Architecture Using Nii Metric Compression
76	2016	An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code
77	2016	Low-Power Parallel Chien Search Architecture Using A Two-Step Approach
78	2016	Fault Tolerant Parallel Ffts Using Error Correction Codes And Parseval Checks
79	2016	Concept, Design, And Implementation Of Reconfigurable Cordic
80	2016	On Efficient Retiming Of Fixed-Point Circuits
81	2016	A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits
82	2016	A High-Performance Fir Filter Architecture For Fixed And Reconfigurable Applications
83	2016	Flexible Dsp Accelerator Architecture Exploiting Carry-Save Arithmetic
84	2016	Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation
85	2016	Pre-Encoded Multipliers Based On Non-Redundant Radix-4 Signed-Digit Encoding
86	2015	Reliable and Error Detection Architectures of Pomaranch for False-Alarm-Sensitive Cryptographic Applications
87	2015	RECURSIVE APPROACH TO THE DESIGN OF A PARALLEL SELF-TIMED ADDER
88	2015	A novel approach to realize Built-in-self-test(BIST) enabled UART using VHDL
89	2015	LOW-POWER AND AREA-EFFICIENT SHIFT REGISTER USING PULSED LATCHES
90	2015	High Speed Convolution And Deconvolution Algorithm Based On Ancient Indian Vedic Mathematics
91	2015	A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler
92	2015	A GENERALIZED ALGORITHM AND RECONFIGURABLE ARCHITECTURE FOR EFFICIENT AND SCALABLE ORTHOGONAL APPROXIMATION OF DCT
93	2015	DESIGN AND IMPLEMENTATION OF AREA-OPTIMIZED AES BASED ON FPGA
94	2015	RECURSIVE APPROACH TO THE DESIGN OF A PARALLEL SELF-TIMED ADDER

95	2015	Energy and Area Efficient Three-Input XOR/XNORs With Systematic Cell Design Methodology
96	2015	RELIABLE AND ERROR DETECTION ARCHITECTURES OF POMARANCH FOR FALSE-ALARM-SENSITIVE CRYPTOGRAPHIC APPLICATIONS
97	2015	A NOVEL AREA-EFFICIENT VLSI ARCHITECTURE FOR RECURSION COMPUTATION IN LTE TURBO DECODERS
98	2015	NON-BINARY ORTHOGONAL LATIN SQUARE CODES FOR A MULTILEVEL PHASE CHARGE MEMORY (PCM)
99	2015	LOW-POWER PROGRAMMABLE PRPG WITH TEST COMPRESSION CAPABILITIES
100	2015	LOW-POWER AND AREA-EFFICIENT SHIFT REGISTER USING PULSED LATCHES
101	2015	A LOW-POWER HYBRID RO PUF WITH IMPROVED THERMAL STABILITY FOR LIGHT WEIGHT APPLICATIONS
102	2015	Area-Efficient Fixed-Width Squarer with Dynamic Error-Compensation Circuit
103	2015	A 28 nm Configurable Memory (TCAM/BCAM/SRAM) Using Push-Rule 6T Bit Cell Enabling Logic-in-Memory
104	2014	A Decimal / Binary Multi-operand Adder using a Fast Binary to Decimal Converter
105	2014	Design and Development of FPGA Based Low Power Pipelined 64-Bit RISe Processor with Double Precision Floating Point Unit
106	2014	Comments on â€œSelf-Checking Carry-Select Adder Design Based on Two-Rail Encodingâ€•
107	2014	A Fully Static Topologically-Compressed 21-Transistor Flip-Flop With 75% Power Saving