High Efficiency Soft-Switching AC-DC Converter with Single-Power-Conversion Method

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***Abstract*— This paper presents a high efficiency isolated ac-dc converter topology. The proposed converter consists of a full-bridge diode rectifier, an isolated resonant dc-dc converter, and only one controller. The proposed converter provides the soft-switching technique for all components operating at high frequency, allowing for an improvement in power density without a cost of power-conversion efficiency. Furthermore, by using a novel control algorithm that controls both power factor and output power, the converter performs ac–dc power conversion in only a single power processing step. These characteristics enable the proposed converter to provide high efficiency, high power density, and a high power factor. A 2 kW prototype was implemented, and its performance and validity were evaluated based on experimental results.**

***Index Terms*— AC-DC power conversion, galvanic isolation, power factor correction, zero-voltage switching, zero-current switching.**

I. INTRODUCTION

WITH an increase in the use of ac–dc converters in various industrial fields, demand for the development of an ac–dc converter with high efficiency and high power density has increased. Traditionally, ac–dc converters with a two-stage circuit configuration have been widely used [1]-[3]; they consist of an ac–dc converter with power factor correction (PFC) [4], [5] followed by an isolated dc–dc converter [6]-[9] and provide nearly unity power factor and reliable output regulation. In [3], a two-stage ac–dc converter employing an interleaved boost PFC converter and an LLC resonant converter was introduced. Because the converter increases the effective switching frequency using the interleaved technique and employs soft-switching operation of all components in the dc–dc stage, it improves both efficiency and power density. However, conventional two-stage converters, including the converter introduced in [3], have inherently high circuit owing to their two-stage complexity and low efficiency circuit configuration.

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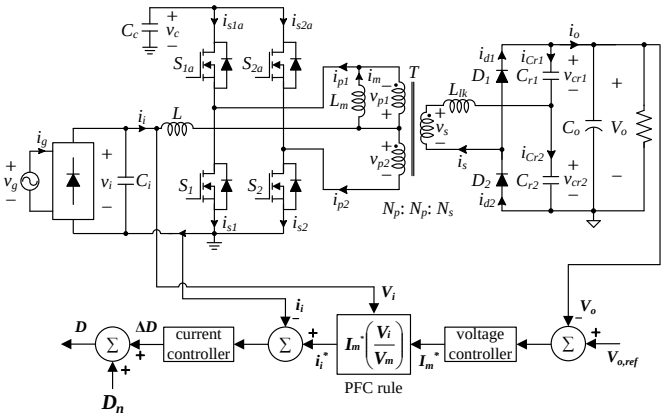


Fig. 1. Circuit configuration and control block diagram of the proposed converter.

The single-stage circuit configuration is an alternative that may overcome the drawbacks of the conventional two-stage converters [10]-[15]. Single-stage converters have been developed based on various converter topologies involving, e.g., a flyback, a forward converter, and a full-bridge converter. Such converters are simpler and more cost-effective than two-stage ac–dc converters; however, they suffer from huge switching losses owing to their hard-switching operation. Furthermore, the single-stage approach performs ac–dc power conversion depending on the circuit design without any PFC control, which results in a poor power factor and very large harmonics. In [16], [17], single-stage converters using an additional auxiliary circuit were developed; the use of the additional circuit provides high power factor and power quality, but causes additional power losses and involves a highly complex circuit structure.

This paper presents an ac–dc converter with high efficiency and high power density. The proposed converter consists of a full-bridge diode rectifier, an isolated resonant dc–dc converter, and only one controller. To obtain high power density without a cost of power-conversion efficiency, the proposed converter provides soft-switching for all components operating at high frequency. The proposed converter performs both PFC and output power control in only one power-processing step by using a novel control algorithm; thus, the converter provides high power quality, producing a high power factor and low total harmonic distortion (THD) without requiring a PFC circuit. Overall, the proposed converter has the following advantages:

1) Due to its soft-switching technique and single-power-conversion approach, the proposed converter can achieve high efficiency and high power density.

2) Without an additional circuit, the proposed converter can provide a high power factor using its control algorithm, unlike the converters in [16], [17].

A description of the operation principle and a relevant analysis of the proposed converter are presented in the following section. In Section III, a 2 kW prototype of the proposed converter is implemented and its performance and validity are evaluated based on experimental results.

II. Proposed Soft-switching AC-DC Converter with Single-power-conversion

Fig. 1 shows the circuit configuration and control block diagram of the proposed converter; it consists of a full-bridge diode rectifier, an isolated resonant dc–dc converter, and a controller. As shown in Fig. 1, the proposed converter controls both the input current and the output voltage with only one controller; this is different from conventional single-stage ac–dc converters, which perform only output regulation.

The dc–dc converter is derived from a current-fed push–pull converter. It employs an active-clamp circuit and a series resonant circuit. The active-clamp circuit is composed of the auxiliary switches S_{1a}, S_{2a} and the clamping capacitor C_c. The active-clamp circuit increases conversion efficiency by reducing the switching losses on the switches and by recycling energy stored in the leakage inductance L_{lk}. Moreover, this circuit limits voltage stresses across the switches and avoids damage caused by surge voltage. The series resonant circuit consists of the leakage inductance L_{lk} and a voltage doubler rectifier circuit. This resonant circuit alleviates the reverse recovery problem on the rectifier diodes D_1 and D_2 by providing zero-current switching (ZCS) turn-off for the diodes.

A. Operation Principle

The proposed converter regulates the input current and output power by adjusting the pulse-width-modulation (PWM) signals of the switches. The main switches S_1 and S_2 have the same duty D, and their PWM signals are generated with a 180° phase difference. S_{1a} (S_{2a}) operates complementarily to S_1 (S_2) with a short dead-time.

To analyze the steady-state operation of the proposed converter, several assumptions are made as follows:

1) All switches S_1, S_2, S_{1a}, and S_{2a} are considered to be ideal switches except for their body diodes.
2) As the switching frequency f_s is much higher than the grid frequency f_g, it is assumed that the input voltage V_i is constant during one switching period T_s.
3) For symmetric operation, C_{r1} is identical to C_{r2}.
4) The clamp capacitors C_c and the output capacitor C_o are sufficiently large to make the clamp capacitor voltage V_c and the output voltage V_o constant.
5) The transformer T is composed of an ideal center-tap transformer with the primary winding turns N_p, the secondary winding turns N_s, the magnetizing inductance L_m, and the leakage inductance L_{lk} on the secondary side.

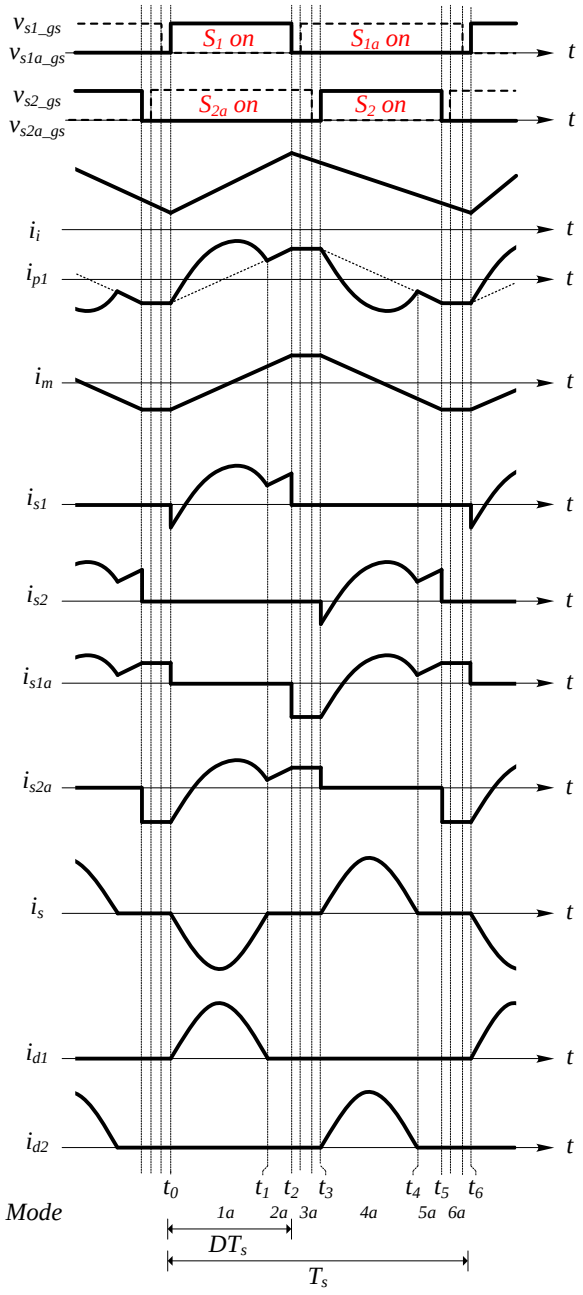


Fig. 2. Key waveforms of the proposed converter for D<0.5.

The operational region is determined by whether or not the duty D is less than 0.5. Figs. 2 and 3 show the theoretical waveforms and the equivalent circuits, respectively, during the half switching period in the region for which D<0.5. In this region, six operational modes exist during one switching period. However, the symmetrical operation of the circuit makes it possible to understand the steady-state operation in this region by analyzing only half a period. Before *Mode 1a*, current i_{p1} flows in the negative direction, and the secondary current i_s remains zero.

Mode 1a [t_0, t_1]: At t_0, the switch S_1 is turned on. At that time, i_{p1} flows through the body diode of S_1, so that S_1 is turned on in the zero-voltage state. During this mode, the primary voltage

v_{p1} is the positive voltage with half of the clamp capacitor voltage, $V_c/2$. The magnetizing current i_m increases as

$$i_m(t) = i_m(t_0) + \frac{V_c}{2L_m}(t - t_0). \tag{1}$$

In this mode, the power is transferred to the output across the transformer. The secondary current i_s flows through D_1, and the state equations are obtained as follows:

$$L_{lk}\frac{di_s}{dt} = nVc - v_{Cr1} \tag{2}$$

$$i_s = C_{r1}\frac{dv_{Cr1}}{dt} - C_{r2}\frac{dv_{Cr2}}{dt} \tag{3}$$

where n is the turns ratio of the transformer and given by $N_s/2N_P$ and v_{cr1} and v_{cr2} are the voltages across C_{r1} and C_{r2}, respectively. As V_o is constant, i_s can be rewritten as

$$i_s(t) = C_{r1}\frac{dv_{cr1}(t)}{dt} - C_{r2}\frac{d(V_o - v_{cr1}(t))}{dt} = C_r\frac{dv_{cr1}(t)}{dt} \tag{4}$$

where the equivalent resonant capacitance C_r is $C_{r1}+C_{r2}$. Using (2) and (4), the voltage v_{Cr1} across C_{r1} and the secondary current i_s are derived as

$$v_{Cr1}(t) = nV_c - (nV_c - v_{Cr1}(t_0))\cos\omega_r(t - t_0) \tag{5}$$

$$i_s(t) = \frac{nV_c - V_{Cr1}}{Z_r}\sin\omega_r(t - t_0) \tag{6}$$

where V_{cr1} is the average voltage of v_{cr1}. The angular resonant frequency ω_r and the characteristic impedance Z_r for the series resonant circuit are given by

$$\omega_r = \frac{1}{\sqrt{L_{lk}C_r}},\ Z_r = \sqrt{\frac{L_{lk}}{C_r}}. \tag{7}$$

Considering that i_L is the sum of the primary currents, and the sum of the magnetomotive forces of all windings is zero, the current i_{s1} flowing through S_1 is calculated as

$$\begin{aligned} i_{s1}(t) = i_{p1}(t) &= \frac{i_L(t)}{2} + \frac{nV_c - V_{Cr1}}{Z_r}\sin\omega_r(t - t_0) \\ &+ i_m(t_0) - \frac{V_c}{2L_m}(t - t_0). \end{aligned} \tag{8}$$

At the end of this mode, the resonance is complete, and the secondary current i_s becomes zero.

Mode 2a [t_1, t_2]: At t_1, the diode current i_{d1} becomes zero, and diode D_1 is turned off with zero current; this means that D_1 does not incur reverse recovery loss. In this mode, i_m still increases linearly as (1) and is equal to i_{p1} because no current flows on the secondary side. In *Modes 1a* and *2a*, the switch S_{1a} is turned off, and its voltage stress is defined as the clamp voltage V_c.

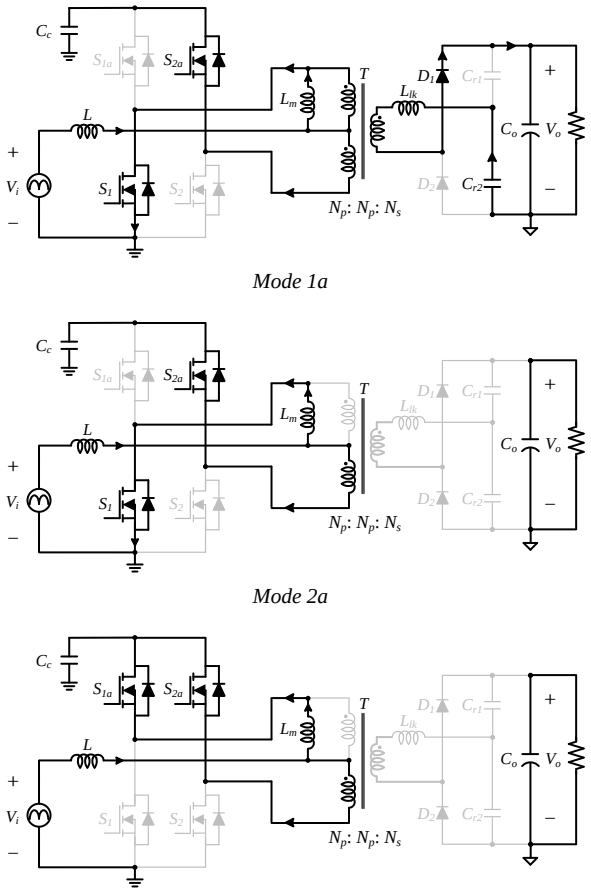


Fig. 3. Equivalent circuits of the proposed converter for D<0.5 during half switching period, $T_s/2$.

The operations in *Modes 4a–6a* for the remaining half period are similar to the respective operations in *Modes 1a–3a*.

From the volt-second balance for L, the clamp capacitor voltage V_c can be derived as

$$V_c = \frac{V_i}{1 - D}. \tag{8}$$

Equation (5) indicates that the average voltage V_{cr1} of v_{cr1} is given by nV_c. Owing to the symmetric operation, the average voltage V_{cr2} of v_{cr2} is also nV_c. The sum of V_{cr1} and V_{cr2} is the output voltage V_o. Thus, the relationship between the input voltage and the output voltage is represented as

$$\frac{V_o}{V_i} = \frac{2n}{1 - D} = \frac{N_s}{N_p}\frac{1}{1 - D} \tag{9}$$

The average value of the secondary current i_s during the half switching period $T_s/2$ is the same as the output current i_o, and can be derived as

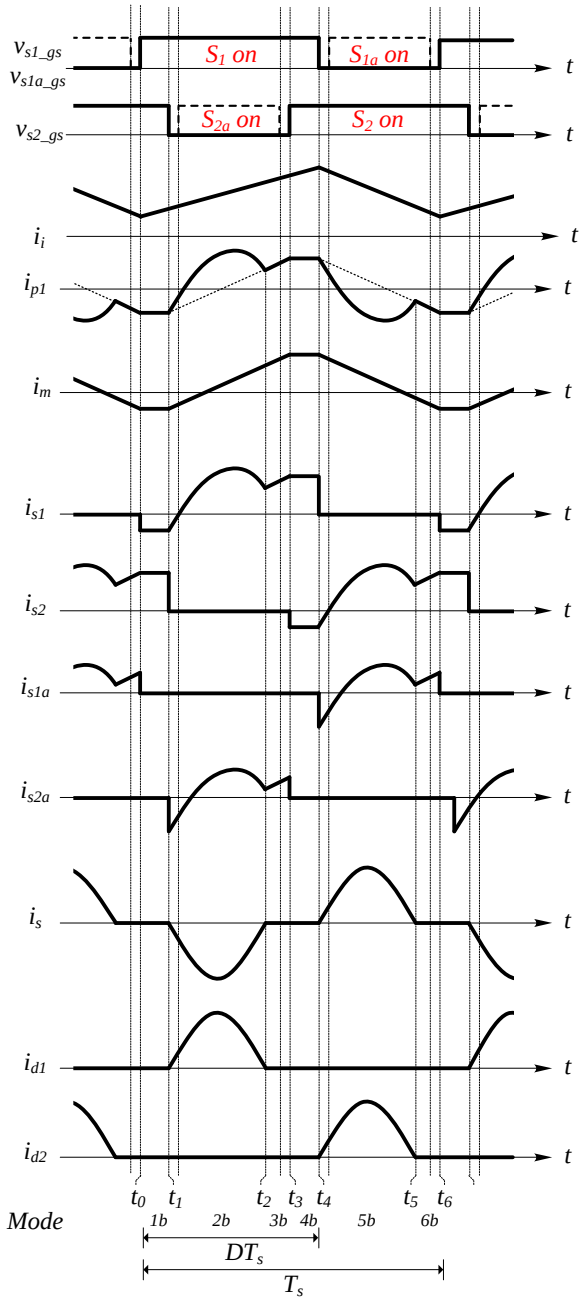


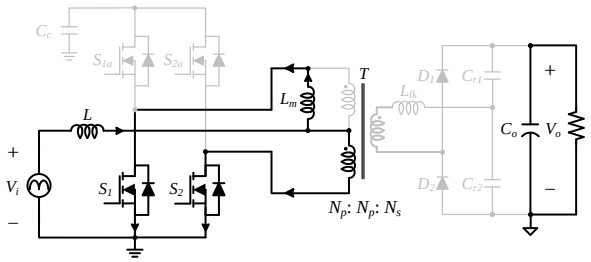
Fig. 4. Key waveforms of the proposed converter for D>0.5.

$$\frac{2}{T_s}\int_{t_0}^{t_1}\frac{I_{s,peak}}{2}\sin\omega_r(t-t_0)dt = i_o \tag{10}$$

where $I_{s,peak}$ is the peak value of i_s over one switching period. From (6) and (10), $I_{s,peak}$ can be obtained as

$$I_{s,peak} = \frac{nV_c - V_{Cr1}}{Z_r} = \frac{\pi\omega_r i_o}{\omega_s} \tag{11}$$

Fig. 4 shows the theoretical waveforms in the region D>0.5. As shown in Fig. 4, when D is greater than 0.5, there is an interval in which the gate signals of the switches S_1 and S_2 are overlapped, as occurs in *Mode 3b*; the equivalent circuit for this



Mode 3b

Fig. 5. Equivalent circuit of the proposed converter for D>0.5 in the overlapped region.

state is shown in Fig. 5. During this interval, voltages v_{p1} and v_{p2} are zero and current i_m is held constant, as in *Mode 3a* for D < *0.5*. Thus, operation in this region is analogous to that of the region for D < 0.5; accordingly, a detailed description is omitted.

B. Control Algorithm for Single-power-conversion method

The proposed converter does not include an additional circuit for PFC. Thus, a control algorithm for both input current and output voltage regulation with only one power-conversion process needs to be incorporated.

According to the switching operation of the main switch, the average voltage equation for the inductor L during half the switching period can be derived as

$$(V_i - \frac{V_C}{2})D + (V_i - V_C)(\frac{1}{2} - D) = L\frac{di_i}{dt} \simeq 2L\frac{\Delta i_i}{T_s} \tag{12}$$

where Δi_i is the input current variation. From (12), the duty D is derived as follows:

$$D = 1 - \frac{N_s}{N_p}\frac{V_i}{V_{o,ref}} + 2L\frac{\Delta i_i}{nV_{o,ref}T_s} = D_n + \Delta D \tag{13}$$

where $V_{o,ref}$ is the reference output voltage. The nominal duty D_n and the feedback control duty ΔD are defined as

$$D_n = 1 - \frac{N_s}{N_p}\frac{V_i}{V_{bat,ref}},\quad \Delta D = 2L\frac{\Delta i_i}{nV_{bat,ref}T_s} \tag{14}$$

Equation (14) indicates that D_n is decoupled from the original nonlinear system in (13), and as a consequence, the relation between ΔD and Δi_i becomes linear. Thus, the nominal duty D_n- contributes to converting the nonlinear system to a first-order linear system, and to alleviating the burden on the feedback controller.

Under a unity power factor, the input voltage V_i and the input current i_i are the absolute values of the grid voltage v_g and the grid current i_g, respectively, and are expressed as

$$V_i = V_m|\sin\omega t|,\quad i_i = I_m|\sin\omega t| \tag{15}$$

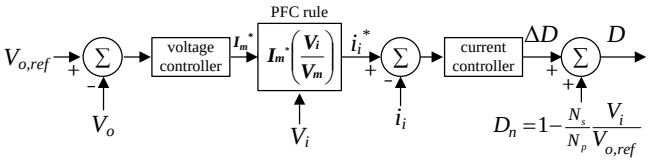


Fig. 6. Proposed control block diagram for the single-power-conversion.

where V_m and I_m are the maximum values of v_i and i_i, respectively, and ω is the angular frequency of the grid. Fig. 6 shows a proposed control block diagram for the single-power-conversion approach. It is seen from the figure that the input current reference i_{i_ref} is derived using knowledge obtained from the input voltage V_i as follows:

$$i_{i\_ref} = I_m^* \left(\frac{V_i}{V_m} \right) \tag{16}$$

where I_m^* is the amplitude of the input current reference. According to the power difference between the input power and output power, the output voltage is decided. If the input power is excessed than the power required from the load, the output voltage increases. On the other hand, the output voltage decreases if the input power is lower than the power required from the load. The voltage controller in Fig. 6 adjusts a value I_m^*, reflecting the input power, so that it eliminates the difference between V_{o_ref} and the sensed output voltage V_o. In the proposed control system, the voltage controller is easily implemented with a proportional-integral controller. To obtain a high power factor, it is necessary to match the phase of the grid current i_g with that of the input voltage v_g. Because the input voltage V_i includes information about the phase of v_g, synchronization with v_g can be achieved using V_i. Thus, without a complex computational burden, an input current reference that is synchronized with v_g can be obtained as (16). The current controller is simply implanted with the proportional controller because its output value ΔD has a linear first-order relation with Δi. Consequently, the duty ratio D is obtained by adding the nominal duty D_n and the feedback control duty ΔD.

C. Design Guideline for soft-switching technique

The soft-switching technique allows the proposed converter to obtain high efficiency and high power density. In this section, the soft-switching conditions for the proposed converter are introduced.

The zero-voltage switching (ZVS) turn-on for S_{1a} and S_{2a} is naturally obtained from the stored energy in L_m and L_{lk}. However, to achieve the soft-switching of the main switches S_1 and S_2, a specific converter design is required. To achieve the ZVS turn-on of S_1 and S_2, the switch currents i_{s1} and i_{s2} should be in the negative direction before each gate signal is transferred to the corresponding switch. Because the average secondary current i_{s_avg} is zero, the average magnetizing current i_{m_avg} is the same as the average current i_{p1_avg} of i_{p1}. Furthermore, because the proposed converter has symmetrical circuit design and operation, the relationship between i_{m_avg} and i_i can be represented as

$$i_{m\_avg} \simeq \frac{i_i}{2}. \tag{17}$$

Assuming that there is no power loss, the instantaneous input power is equal to the instantaneous output power p_o as

$$p_{in} = v_i i_i = V_o i_o = p_o \tag{18}$$

where i_o is the output current. Then, the average current i_{m_avg} in (17) can be re-expressed from (9) and (18) as follows:

$$i_{m\_avg} = \frac{n i_o}{1-D}. \tag{19}$$

At t_0, the current i_{s1} flowing through the main switch S_1 is the magnetizing current i_m. From (9), (18), (19), and the waveforms in Fig. 2 and 4, i_{s1} at t_0 can be derived as

$$\begin{aligned} i_{s1(t_0)} &= i_{m\_avg} - \frac{\Delta i_m}{2} \\ &= \begin{cases} \dfrac{n i_o}{1-D} - \dfrac{V_o D T_s}{4 n L_m}, & \text{for } D < 0.5 \\ \dfrac{n i_o}{1-D} - \dfrac{V_o (1-D) T_s}{4 n L_m}, & \text{for } D \geq 0.5 \end{cases} \end{aligned}. \tag{20}$$

To satisfy the ZVS condition of S_1 in (20), the switch current i_{s1} should be negative at t_0. Then, L_m can be designed to meet all operating points within the grid period as

$$L_m \leq \frac{{V_o}^2 D_{\min} (1 - D_{\min})}{4 n^2 f_s p_{o,peak}} \tag{21}$$

where D_{min} is the minimum duty, f_s is the switching frequency, and $p_{o,peak}$ is the peak instantaneous output power at a certain average power level. Due to the symmetrical operation, the ZVS condition for S_2 is equal to that of S_1 as (21).

To achieve the ZCS turn-off of D_1 and D_2, the half resonant period should meet the following conditions as

$$\begin{cases} \dfrac{\pi}{\omega_r} < D T_s, & \text{for } D<0.5 \\ \dfrac{\pi}{\omega_r} < (1-D) T_s, & \text{for } D \geq 0.5 \end{cases}. \tag{22}$$

Equation (22) indicates that D_1 and D_2 are turned off with the zero current at all operating points for D<0.5 if the resonant frequency is greater than the switching frequency. On the other hand, the ZCS region for D>0.5 is determined according to the design of the equivalent resonant capacitor C_r as

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TABLE I
PARAMETERS AND COMPONENTS OF THE PROTOTYPE

Parameters	Symbols	Value
Grid voltage	v_g	120-240V_{rms}
Grid frequency	f_g	60Hz
Output voltage	V_o	360V
Switching frequency	f_s	70kHz
Primary winding turns	N_p	24turns
Secondary winding turns	N_s	20turns
Magnetizing inductance	L_m	88μH
Leakage inductance	L_{lk}	0.5μH
Input inductor	L	0.8mH
Input capacitor	C_i	1μF
Clamp capacitor	C_c	4.4μF
Resonant capacitors	C_{r1}, C_{r2}	2μF
Output capacitor	C_o	680μF
Components	**Symbols**	**Part**
Switches	S_1, S_2, S_{1a}, S_{2a}	FCA76N60N
Output diodes	D_1, D_2	BYV34X-600
Bridge diode on the grid side	-	KBPC3506

$$C_r < \frac{1}{\omega_{rc}^2 L_{lk}} \tag{23}$$

where the critical angular resonant frequency ω_{rc} is defined as $\pi f_s/D_{cri}$, where the critical duty D_{cri} is the maximum duty in the ZCS region. Fig. 7 shows the critical resonant capacitor C_r for satisfying the ZCS turn-off of D_1 and D_2 in accordance with the duty variation.

III. EXPERIMENTAL RESULTS

To evaluate the feasibility of the proposed converter, a 2kW prototype was built and tested. The grid voltage range was from 120 to 240V_{rms}, and the nominal grid voltage was set to 220V_{rms}. The reference of the output voltage was designated as 360V. To produce a minimum duty D_{min} of about 0.2, the turns ratio n was set as 20/48. Then, considering the ZVS condition in (21), the magnetizing inductance L_m was determined to be 80μH. The resonant capacitors C_{r1} and C_{r2} were selected based on the ZCS condition of the diodes in (23), with each corresponding value equal to 2μF. The major experimental parameters for the prototype are listed in Table I. The control algorithm in Fig. 6 was digitally implemented using a single DSP chip, dsPIC33EP512GM604 (Microchip), which was responsible for providing gate signals and sensing the current and voltage with 12bit A/D conversion.

Fig. 8 shows the grid voltage v_g and the grid current i_g. It is seen that i_g is a nearly perfectly sinusoidal and in phase with v_g. In this case, the power factor is measured to be 0.999.

Figs. 9 and 10 show the soft-switching techniques on the proposed converter. As shown in Fig. 9, the current i_{s1} (i_{s1a}) begins to flow through the body diode of the switch S_1 (S_{1a}) with a negative value, and the voltage become zero. It is clear

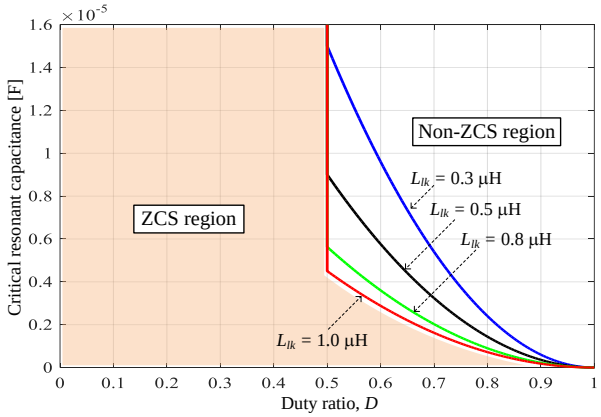


Fig. 7. ZCS region of the proposed converter according to circuit design.

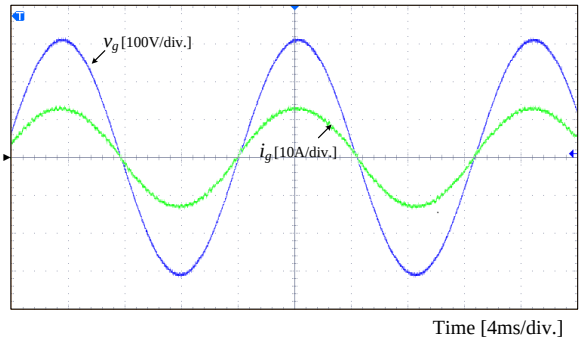
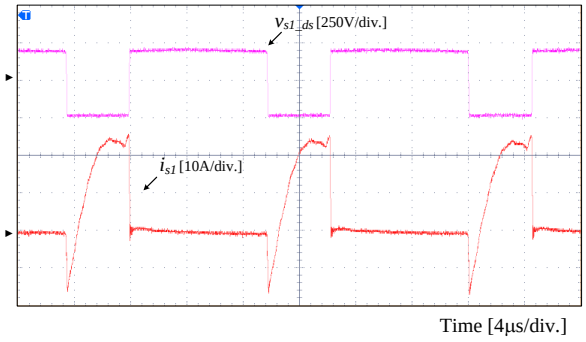
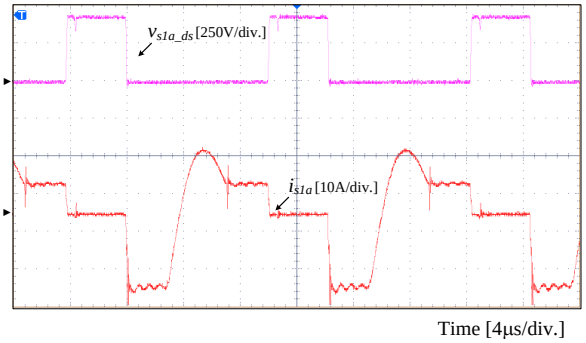


Fig. 8. Experimental waveforms for the grid voltage v_g and the grid current i_g.



(a)



(b)

Fig. 9. Experimental results for the soft-switching technique on the switches (a) Drain-to-source voltage v_{s1_ds} and switch current i_{s1} of the main switch S_1. (b) Drain-to-source voltage v_{s1a_ds} and switch current i_{s1a} of the active-clamp switch S_{1a}.

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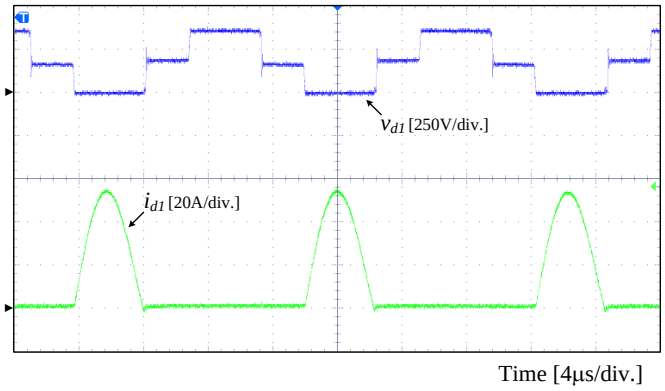

Fig. 10. Experimental results for the soft-switching technique on the output diode D_1.

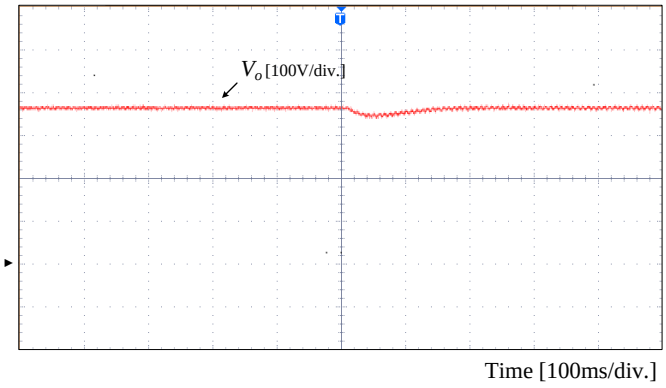

Fig. 11. Experimental result for the output voltage under the load variation.

that all switches perform the ZVS turn-on. In addition, the voltage stress of each switch is defined as a constant voltage V_c; it is possible by the active-clamp circuit which prevents huge voltage stress. In the secondary side, as shown in Fig. 10, the diode current i_{d1} become zero before the diode D_1 is turned off. Thus, it is expected that the proposed converter can reduce the switching losses on all components that operate at high frequency through its soft-switching techniques.

Fig. 11 shows the experimental result for the output voltage variation under load variation from the full load to the quarter load. This result demonstrates that the voltage controller in Fig. 6 makes the output voltage V_o track its reference 360V quickly despite of the load variation.

Fig. 12 shows the measured power factor as a function of the input voltage level. The power factor is greater than 0.99 over the entire voltage range, which indicates that the proposed converter can achieve a high power factor without requiring an additional circuit for PFC.

Fig. 13 shows an efficiency comparison with conventional converter topologies. It is seen that the proposed converter has higher efficiency than the other converter topologies over the entire range of load conditions. In the proposed converter, the maximum efficiency are the rated efficiency are measured to be 96.4% and 96.1%, respectively.

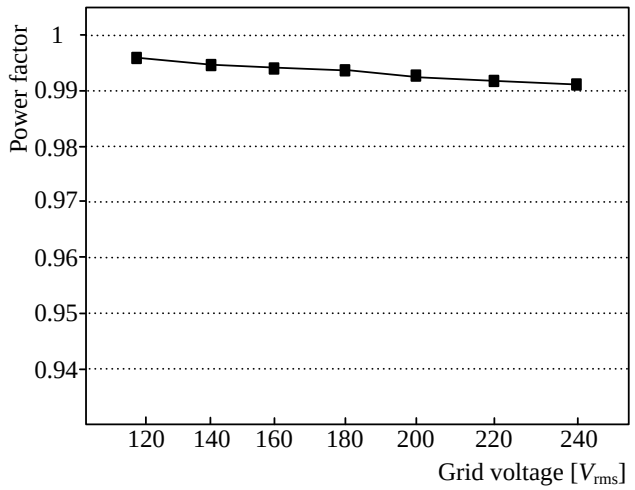

Fig. 12. Measured power factor according to the grid voltage level.

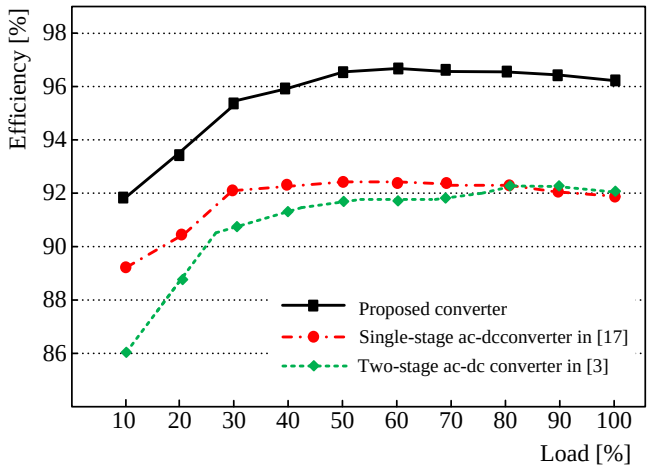

Fig. 13. Efficiency comparison according to the converter topology.

IV. Conclusion

A novel ac–dc converter topology with high efficiency and high power density was introduced and analyzed. The proposed converter employs soft-switching techniques and a single-power-conversion method, which together contribute to improving the power-conversion efficiency and power density. The proposed converter uses a control algorithm that enables it to perform both PFC and output power control without the use of a complex circuit structure or the need for several power-conversion steps. Because of these advantages, the proposed converter is suitable for use in industrial applications that require high efficiency and high density. To validate the proposed converter, a 2 kW prototype was built and tested. The experimental results indicate that the proposed converter achieves a high efficiency of 96.1% over the full range of load conditions and provides a power factor of nearly unity over the entire input voltage range.

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