Series Compensator Based on Cascaded Transformers Coupled with Three-Phase Bridge Converters

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***Abstract*—This paper proposes a multilevel series compensator (MSC) to deal with: i) voltage sags/swells, ii) harmonic compensation or iii) reactive power compensation. Such a device can be considered as a dynamic voltage restorer (DVR) or a series active power filter (Series-APF). The MSC can improve the power-quality of loads located in stiff systems. The configuration is based on three-phase bridge (TPB) converters connected by means of cascaded single-phase transformers. This arrangement permits to use a single dc-link. A generalization for K-stages in which K-transformers are coupled with K-TPB converters, is presented. The topology permits to generate a high number of levels in the voltage waveforms with a low number of power switches. The multilevel waveforms are generated by the converters through a suitable PWM strategy that takes into consideration the transformer turns ratios. Modularity and simple maintenance makes proposed MSC an attractive solution compared to some conventional configurations. Model, PWM strategy and overall control are discussed in this paper. Simulation and experimental results are presented.**

I. Introduction

Distribution power systems are suffering hard impact in their power-quality. This is due to the intensive use of non-linear loads added with growth of renewable energy sources. Such aspects have been leading electrical power system to poor power-quality levels. Most common disturbances include: i) harmonic voltages/currents, ii) voltages imbalances, iii) voltage sags/swells, iv) flickers, v) transients and vi) interruptions. Among them, voltage sags are considered as most important power-quality problem and are attracting quite large amount of attention in the literature [1]–[3]. To mitigate voltage disturbances at the grid, some custom power devices have been introduced and investigated. For instance, dynamic voltage restorer (DVR) [4], [5], series active power filter (Series-APF) [6], [7] and unified power-quality conditioner (UPQC) [8], [9]. These three options satisfy the series voltage compensation criteria. However, each of them present particularities on their application field. UPQC is attractive to compensate both voltage and current disturbances by using series and shunt converters [10]. If the DC energy storage unit is not a critical issue for the compensator design, DVRs should be suitable due to short time operation feature [11]. On the other hand, series-APF can operate without a DC source connected in the dc-link. In this case, the dc-link regulation strategy must be considered for a satisfactory operation [11], [12].

The series compensator (DVR or Series-APF) is commonly composed by: i) injection transformers, ii) voltage source converter (VSC), iii) energy storage, iv) optional passive filters and v) protection circuits (e.g., bypass thyristors). The VSC based on two-level (2L) converter is commonly used for low voltage systems. When the application needs higher voltage level (i.e., high power applications), the multilevel based on VSC becomes a more attractive solution [4]. In this way, some multilevel configurations have been investigated in the technical literature [4], [13]–[15]. However, those multilevel configurations have some issues associated to the high number of dc-link capacitors, inherent in their topology. For instance, cascaded neutral point-clamped (NPC) and cascaded flying capacitors have issues with imbalance dc-link voltages and power sharing in each cell [16]. In addition, the lifetime of dc-link capacitors stands out as one of the most important issues in terms of failure rate at the operation of power electronic systems [17]–[19]. Then, a high number of dc-link capacitors increases the failure probability of the topology.

To cope with this issue, the concept of using cascaded transformers have been introduced as one alternative solution [20], [21]. In this way, the multilevel features can be guaranteed by using a single dc-link capacitor in its configuration. A conventional DVR based on cascaded transformer coupled with H-bridge (HB) converters was presented in [4]. Usually, injection transformers are taken into consideration at the series voltage compensator design [22]. In this way, the transformer turns ratio associated with each transformer can be considered to

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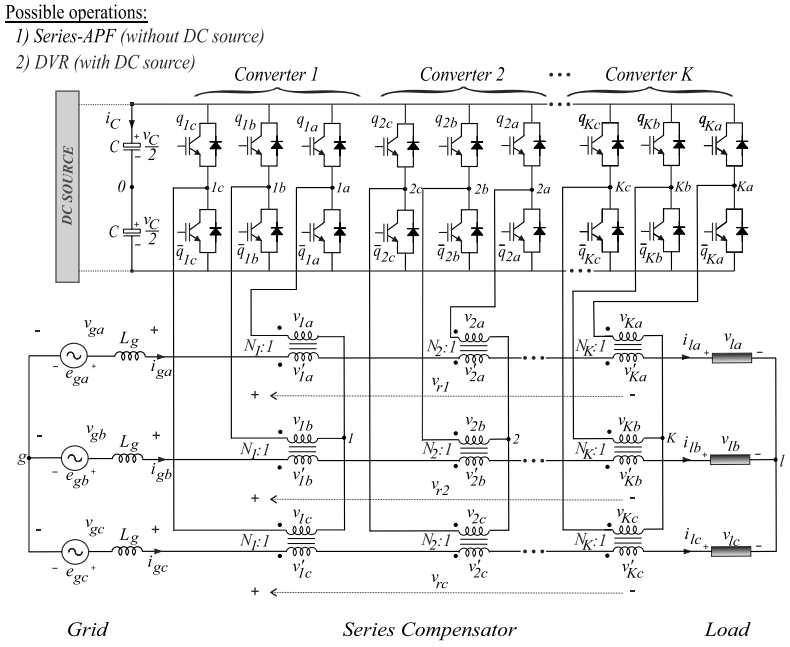

Figure 1. Proposed series compensator. Generalization with K-stages (i.e., K-cascaded transformers and K-TPB converters).

improve the waveform quality of the output voltage generated by the compensator. This paper proposes a series compensator based on cascaded transformers coupled with three-phase bridge (TPB) converters, see Fig. 1. Equivalent multilevel operation is achieved with reduced number of semiconductors devices in comparison with conventional HB. The multilevel waveforms are generated by TPB converters through a suitable PWM strategy associated with the transformer turns ratio. The modularity and simple maintenance make proposed MSC an attractive solution in comparison with some conventional configurations. The model and control are addressed in this paper. Simulation and experimental results are presented too.

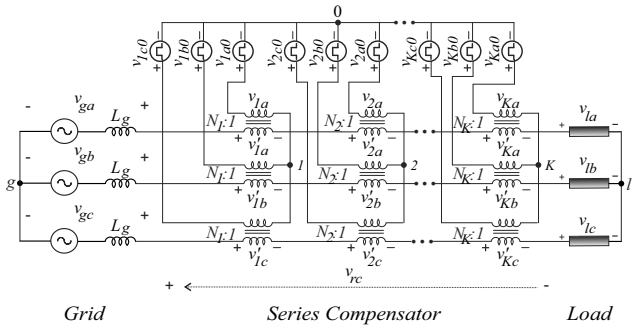

Figure 2. Ideal equivalent circuit for generalized proposed MSC.

II. Proposed MSC model

The configuration depicted in Fig. 1 is generalized for K-stages (i.e., K-transformers and K-three-phase-bridge converters). The converters leg are represented by K-power switches (i.e., q_{1j}, $\overline{q}_{1j}$, q_{2j}, $\overline{q}_{2j}$, ..., q_{Kj}, and $\overline{q}_{Kj}$) in which the subscript j is related for each phase (e.g, $j = a, b, c$). In addition, power switches q and $\overline{q}$ are complementary from each other. The conduction state of all power switches is represented by an

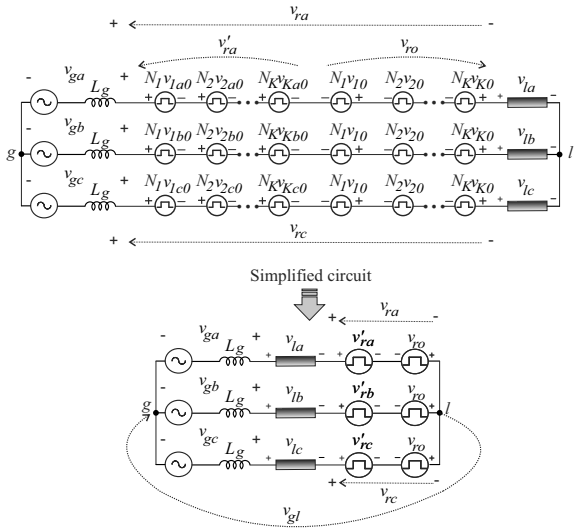

Figure 3. Equivalent simplified circuit. Modified (on the top). Simplified (on the bottom).

homonymous binary variable, where $q = 1$ indicates a closed switch while $q = 0$ an open one.

The configuration model becomes simple when its ideal equivalent circuit, see Fig. 2, is considered. In this way, the converter pole voltages (v_{1j0}, v_{2j0},..., v_{Kj0}), can be expressed as

$$v_{kj0} \quad = \quad (2q_{kj} - 1)\frac{v_C}{2} \tag{1}$$

where k corresponds for each stage (i.e., $k = 1, 2, 3, ..., K$), j is related for each phase ($j = a, b, c$) and v_C is the dc-link voltage.

The voltages at the primary side of the injection transform-

ers for each phase are expressed as

$$v_{ka} = v_{ka0} - v_{k0} \quad (2)$$

$$v_{kb} = v_{kb0} - v_{k0} \quad (3)$$

$$v_{kc} = v_{kc0} - v_{k0} \quad (4)$$

The system model considering the grid voltages (v_{gj}), transformer voltages at the secondary side ($v_{1j}^{'}$, $v_{2j}^{'}$, ..., $v_{Kj}^{'}$) and load voltages (v_{lj}) can be expressed as

$$v_{gj} = (v_{1j}^{'} + v_{2j}^{'} + ... + v_{Kj}^{'}) + v_{lj} - v_{gl} \quad (5)$$

where $v_{1j}^{'} = N_1(v_{1j0} - v_{10})$, $v_{2j}^{'} = N_2(v_{2j0} - v_{20})$, ..., $v_{Kj}^{'} = N_K(v_{Kj0} - v_{K0})$ in which N_1, N_2, ..., N_K are the transformer turns ratios associated with converters 1, 2,..., K, respectively.

A simplified circuit can be obtained from that one in Fig. 2 by considering perfect isolation from primary to secondary side of the transformers (i.e., ideal transformers), see Fig. 3. Such an equivalent circuit permits to clarify the approach used to write the following equations. It should be noticed that the output voltages (v_{rj}) of the resultant converter can be expressed as

$$v_{rj} = v_{rj}^{'} - v_{ro} \quad (6)$$

$$v_{rj}^{'} = N_1 v_{1j0} + N_2 v_{2j0} + ... + N_K v_{Kj0} \quad (7)$$

$$v_{ro} = N_1 v_{10} + N_2 v_{20} + ... + N_K v_{K0}. \quad (8)$$

From (8) and (5) the system model is simplified as

$$v_{gj} - v_{lj} = v_{rj}^{''} = v_{rj}^{'} - v_{ro} - v_{gl}. \quad (9)$$

The voltages v_{rj} can have a maximized number of levels if the voltages ($v_{rj}^{'}$) assume a suitable sequence of the switching states. This is achieved by considering the transformer turns ratios (N_1, N_2, ..., N_K). Table I shows a particular case, with 3 transformers per phase and 3 three-phase-bridge (TPB) converters, in which the voltage $v_{rj}^{'}$ can reaches 8 different levels per phase according to the switching states. In this case, the compensator must operate with different transformer turns ratios (e.g., $N_k = 2^{(k-1)}$). It can be seen that these ratios provide the best (higher) number of voltage levels (symmetrically spaced) from each other. Fig. 4 presents an one-dimension region of output voltage $v_{rj}^{'}$ for each phase (e.g., $j = a, b, c$) associated with switching states [q_{1j}, q_{2j} and q_{3j}]. Such a representation permits to easily synthesize the reference output voltage by using always the nearest switching states to the reference output voltage. This approach is similar to that one presented in [23] and has advantages to reduce the switching losses of the power converter topology.

Table II shows the generalization for K-transformers and K-TPB converters. The respective levels disposition in one-dimension region is presented in Fig. 5. Notice that the transformer turn ratios follows a geometric sequence with ratio equal to 2 (e.g., $N_1 = 1$, $N_2 = 2$, $N_3 = 4$, $N_4 = 8$, $N_5 = 16$, ..., $N_K = 2^{(K-1)}$) that gives always the best option in terms of:

i) maximum number of levels generated at the voltage $v_{rj}^{'}$;

ii) symmetrical dv/dt at v_{rj} from one level to the other.

Table I
VARIABLES FOR RESULTANT CONVERTER WITH 3 CASCADED TRANSFORMERS PER PHASE AND 3 TPB CONVERTERS IN WHICH $N_1 = 1$, $N_2 = 2$ AND $N_3 = 4$.

State	Leg state			Output voltage
	q_{3j}	q_{2j}	q_{1j}	$v_{rj}^{'}$=$N_1 v_{1j0}$+$N_2 v_{2j0}$ + $N_3 v_{3j0}$
-7	0	0	0	$-7v_C/2$
-5	0	0	1	$-5v_C/2$
-3	0	1	0	$-3v_C/2$
-1	0	1	1	$-v_C/2$
1	1	0	0	$v_C/2$
3	1	0	1	$3v_C/2$
5	1	1	0	$5v_C/2$
7	1	1	1	$7v_C/2$

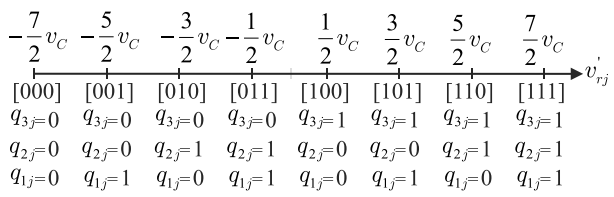

Figure 4. One-dimension of output voltage ($v_{rj}^{'}$) levels region for 3-stages (i.e., $K = 3$ that means $N_1 = 1$, $N_2 = 2$ and $N_3 = 4$).

It should be noted that in this case there is no redundant levels and the switching states will present always maximized number of different levels (i.e., 2^K). If the redundancy is a priority, at least one of the transformer turns ratios must be equal. For instance, $N_1 = 1$ and the others $N_2 = N_3 = ... = N_{(K-1)} = N_K = 2^{(K-1)}$.

Table II
VARIABLES FOR RESULTANT CONVERTER WITH K-CASCADED TRANSFORMERS PER PHASE AND K-TPB CONVERTERS WITH $N_K = 2^{(K-1)}$, VALID FOR $K \geq 3$.

State	Leg state			Output voltage
	q_{Kj}	...	q_{1j}	$v_{rj}^{'}$=$N_1 v_{1j0}$+$N_2 v_{2j0}$ +...+ $N_K v_{Kj0}$
-(2^K-1)	0	...	0	$-(2^K - 1)v_C/2$
-(2^K-3)	0	...	1	$-(2^K - 3)v_C/2$
-(2^K-5)	0	...	0	$-(2^K - 5)v_C/2$
⋮	⋮	⋯	⋮	⋮
-1	0	...	1	$-v_C/2$
1	1	...	0	$v_C/2$
⋮	⋮	...	⋮	⋮
2^K-5	1	...	1	$(2^K - 5)v_C/2$
2^K-3	1	...	0	$(2^K - 3)v_C/2$
2^K-1	1	...	1	$(2^K - 1)v_C/2$

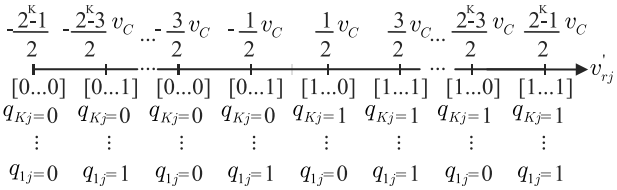

Figure 5. One-dimension of output voltage ($v_{rj}^{'}$) levels region for K-stages (i.e., that means $N_1 = 1$, $N_2 = 2$, $N_3 = 4$, ..., $N_K = 2^{(K-1)}$).

III. PWM Strategy

The pulse width modulation (PWM) technique used in this work is based on level-shifted-carrier-based PWM (LSPWM). However, a simpler algorithm calculation can be obtained. It takes into consideration references for the resultant output voltage ($v_{rj}^{*'}$).

Considering that a voltage controller will provide references for the resultant converter ($v_{rj}^{*''} = (v_{gj} - v_{lj})^*$), the references $v_{rj}^{*'}$ become

$$v_{rj}^{*'} = v_{rj}^{*''} + v_{rogl}^{*} \tag{10}$$

with $v_{rj}^{*'} = v_{1j}^{*'} + v_{2j}^{*'} + ... + v_{Kj}^{*'}$ and v_{rogl}^{*} is a degree of freedom from the system characteristics.

The reference voltage for v_{rhom}^{*} is calculated as

$$v_{rogl}^{*} = \mu_{rogl}^{*} v_{rogl\,\max}^{*} + (1 - \mu_{rogl}^{*}) v_{rogl\,\min}^{*} \tag{11}$$

where $0 \leq \mu_{rhom} \leq 1$ and

$$v_{rogl\,\min}^{*} = -0.5 v_C^{*}(N_1 + ... + N_K) - \min\{v_{rj}^{*''}\} \tag{12}$$

$$v_{rogl\,\max}^{*} = 0.5 v_C^{*}(N_1 + ... + N_K) - \max\{v_{rj}^{*''}\}. \tag{13}$$

Once voltages $v_{rj}^{*''}$ (i.e., $v_{r1}^{*''}$, $v_{r2}^{*''}$ and $v_{r3}^{*''}$) are given from the controller, the algorithm to calculate $v_{rj}^{*'}$ is summarized in following steps:

Step 1) calculate the $v_{rogl\,\min}^{*}$ and $v_{rogl\,\max}^{*}$ values according to (12) and (13);

Step 2) choose μ_{rogl}^{*} between 0 and 1;

Step 3) determine v_{rogl}^{*} from (11);

Step 4) calculate $v_{rj}^{*'}$ from (10).

In this way, the reference voltages $v_{rj}^{*'}$ are compared with $2^n - 1$ triangular waveforms, which are level-shifted carriers (v_{t1} - v_{t2^n-1}) placed according to the levels shown previously in Table II. The result of this comparison gives the switching states (q_{1j}, q_{2j}, ..., q_{Kj}) that are imposed for each TPB converter. Fig. 6 summarizes each step for this PWM strategy.

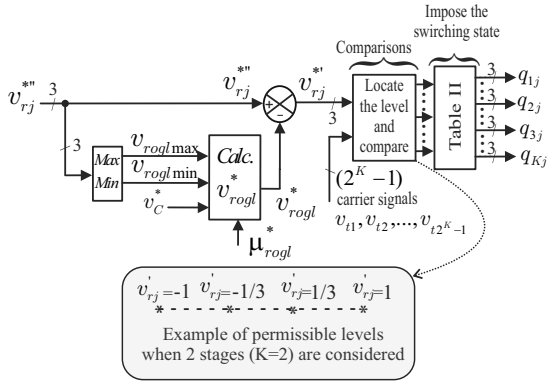

Figure 6. PWM block diagram of generalized proposed MSC. Example of permissible levels were normalized by $v_C/2$.

IV. Control strategy

Fig. 7 shows the control strategy of proposed MSC. Notice that there are two options of operation: 1) as a harmonic series active power filter (Series-APF) or 2) as a dynamic voltage restorer (DVR). The first option regulate the dc-link voltage v_C by means of a conventional PI controller. Such a controller is represented through the block R_C in which gives an small amplitude reference of the resultant voltage to be compensated ($V_r^{*''}$). The block $Gen - v_r$ generate small reference voltages $v_{rjf}^{*''}$ (at the fundamental frequency) synchronized with e_{gj} through the phase-locked-loop (PLL). These small signals are subtracted from the harmonic voltage signals $v_{rjh}^{*''}$ to be compensated furnishing voltage $v_{rj}^{*''}$. More details about this control approach is observed in [7]. In the second option there is only controller R_v in which its input signals are the grid voltages (v_{gj}) and reference load voltages v_{lj}. The output of controller R_v gives reference voltages $v_{rj}^{*''}$ for the PWM strategy. In that figure the switch SW indicates the selection of series APF or DVR operation.

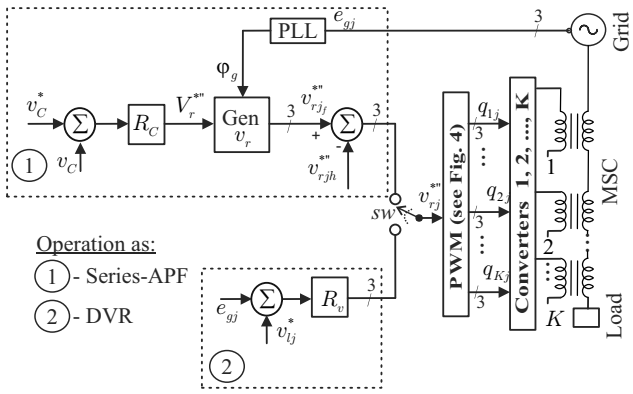

Figure 7. Control block diagram of proposed MSC. Operation as Series-APF (1) or DVR (2).

V. Number of levels per power switch

This feature gives an idea of the cost-benefit associated with the studied topology. For example, let's assume the case with the same number of power switches utilization for both proposed MSC and conventional HB [4] configurations (i.e., 4 power switches per phase). In this case, the proposed MSC will have $K = 2$ with transformer turns ratios $N_1 = 1$ and $N_2 = 2$ while the conventional HB will have $N_1 = 1$. The number of levels generated at $v_{rj}^{'}$ per phase with proposed configuration will be 4 ($3v_C/2$, $v_C/6$, $-v_C/6$ and $-3v_C/2$) whereas the conventional with HB will provide 3 levels (v_C, 0 and $-v_C$). Then, taking into consideration the number of levels divided by the number of power switches used, we will have:

- Proposed MSC
  Number of levels per power switches: $\frac{4}{4} = 1.00$
- Conventional with HB [4]
  Number of levels per power switches: $\frac{3}{4} = 0.75$

Considering 8 power switches per phase, the proposed MSC will have $K = 4$ with transformer turns ratios equal to $N_1 = 1$, $N_2 = 2$, $N_3 = 4$ and $N_4 = 8$. The conventional HB will have a maximized number of level with transformer turns ratios equal to $N_1 = 1$, $N_2 = 3$. Then, the number of levels that can be generated at the output voltage $v_{rj}^{'}$ in one phase is 16 for proposed MSC and 9 for conventional HB. Then, if we divide this by the number of power switches used we find:

- Proposed MSC
  Number of levels per power switches: $\frac{16}{8} = 2.00$
- Conventional with HB [4]
  Number of levels per power switches: $\frac{9}{8} = 1.13$

It can be seen that proposed configuration presents a better performance if compared to conventional with HB, considering this characteristic. Hence, such an improvement is close to 33% (1/0.75) in the first case (with 4 power switches) while the second case (with 8 power switches) will be 76.99% (2/1.13). Then, it permits to observed that this features (i.e., the improvement) increases with the raise of power switches considered for the configurations. Note that the proposed topology uses more transformers. However these transformers have smaller rated power than those used in conventional HB topology.

VI. Topological comparison

A topological comparison among proposed MSC (TPB) and conventional HB is presented in Table III. It can be seen that proposed MSC has lower power switches in comparison with conventional one.

Table III
Device count comparison with the same number of stages (K).

Main devices	Conventional HB [4]	Proposed TPB
Transformers	$3K$	$3K$
IGBTs	$12K$	$6K$
Capacitors	1	1
Levels/phase	3^K	2^K

VII. Harmonic Distortion evaluation

The weighted total harmonic distortion (WTHD) of the resultant voltages (v_{rj}) in the proposed MSC have been computed by using

$$WTHD(p) = \frac{100}{a_1}\sqrt{\sum_{i=2}^{p}\left(\frac{a_i}{i}\right)^2} \tag{14}$$

where a_1 is the amplitude of the fundamental voltage, a_i is the amplitude of i^{th} harmonic and p is the number of harmonics taken into consideration.

Then, considering a maximum injection of v_{rj} and a balanced system, the WTHD of the voltages v_{rj} for proposed configuration can be observed in Table IV. In this result, the switching frequency (f_s) is fixed in 10 kHz. The stages means the number of transformers and three-phase bridge converters used per phase. For example, 2 stages means that proposed MSC operates with 2 transformers and 2 three-phase bridge converters in each phase.

It can be seen in Table IV that as expected the WTHD value decreases with increasing of stages used in proposed MSC. The waveforms for that result, with 2 and 3 stages, are shown in Figs. 8 and 9, respectively.

Table IV
WHTD for proposed MSC in which the stages means the number of transformers and three-phase bridge converter per phase.

Proposed MSC	Transformer turns ratios	WTHD (%)
1 stage	1:1 ($N_1 = 1$)	0.200
2 stages	1:1 ($N_1 = 1$) 2:1 ($N_2 = 2$)	0.055
3 stages	1:1 ($N_1 = 1$) 2:1 ($N_2 = 2$) 4:1 ($N_3 = 4$)	0.023

VIII. Semiconductor losses estimation

In this paper, the power switch losses estimation for proposed MSC and conventional HB was implemented by using the thermal module, an existing tool in PSIM $v9.0$. Such a tool was used with calibration parameters that gives an equivalent loss estimation to that in [24] that was obtained through regression model, achieved by experimental tests. The power switch losses model includes:

a) IGBT and diode conduction losses;
b) IGBT turn-on losses;
c) IGBT turn-off losses;
d) Diode turn-off energy.

Table V shows a comparison between the conventional (based on HB converter [4]) and proposed configuration that uses TPB converter. In this case the same number of power switches (i.e., 6 IGBTs) was fixed for both configurations. Additionally, the same WTHD (e.g., 21 %) value was imposed for both conventional and proposed configurations. This was achieved by fixing the WTHD in 0.21 % for conventional configuration that was obtained with sampling frequency equal to 7.5 kHz. To obtain the same WTHD value by using proposed configuration the frequency was decreased up to 3.3 kHz. Hence, it can be observed the reduction in the switching losses estimation. Once both configurations operates under virtually the same ratings of voltage and current, the conduction losses estimations are close from each other. This leads one to conclude that proposed MSC operates with lower losses if compared to conventional one. The losses reduction is close to 50%. Perhaps, such a reduction compensates the losses of an additional transformer per phase that is needed for proposed configuration operates with 2 stages.

Table V
Losses comparison between proposed MSC operating with 2 stages ($N_1 = 1$ and $N_2 = 2$) and conventional HB with 1 stage.

Configuration		Semiconductor Losses Estimation		
Topology	Stages	Switching	Conduction	Total
Conventional HB	1	540 W	250 W	790 W
Proposed TPB	2	130 W	250 W	380 W

IX. Simulation results

Simulation results through PSIM $v9.0$ are shown in Figs. 8 and 9. Such outcomes show resultant voltage of the converter (v_{ra}), in one phase, a with PWM implementation accordingly to the PWM strategy presented earlier. Figs. 8(a) and 8(b) consider only converters A and B with 2 single-transformers connected in each phase. It can be seen that the result presented in Fig. 8(a) is equivalent to that obtained with 3L-NPC converter or cascaded HB with equal dc-link voltages. Fig. 9 shows implementation with converters 1, 2 and 3 as well as transformers turns ratio being $N_1 = 1$, $N_2 = 2$ and $N_3 = 4$. The result for the other phases is similar.

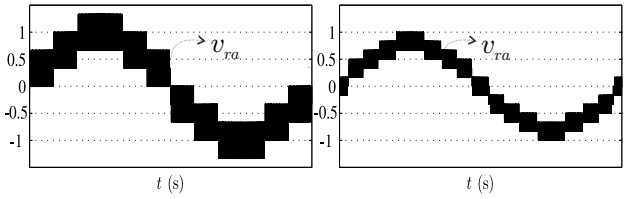

Figure 8. Simulation results. Resultant phase-voltage (v_{ra}) in phase a in which proposed MSC has two TPB converters. (a) Transformer turns ratios being equal to $N_1 = N_2 = 1$. (b) Transformer turns ratios being equal to $N_1 = 1$ and $N_2 = 2$.

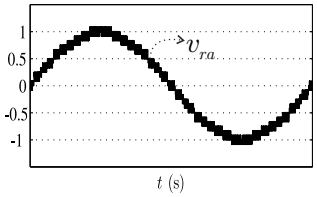

Figure 9. Simulation results. Resultant phase-voltage (v_{ra}) in phase a when proposed MSC has three TPB converters. Transformer turns ratios being equal to $N_1 = 1$, $N_2 = 2$ and $N_3 = 4$.

X. Experimental results

The studies and simulated results of proposed MSC were validated with some experimental tests. The main components of experimental setup are inverters composed by IGBTs from Semikron SKM50GB123D with drivers SKHI23 that are linked with the control strategy by means of a digital processor signal (DSP) TMS320F28335 with microcomputer equipped with appropriated plug-in boards and sensors. The dc-link capacitor considered for the setup was $C = 2200\mu F$ and the switching frequency for the power switches was considered as $f_{sw} = 10kHz$. A photograph of the main devices of this downscaled experimental prototype can be observed in [25].

The dynamic operation of the MSC operating as a Series-APF or as a DVR has been verified. The implementation for this dynamic operation considering two options of operation (i.e., as a series-APF or as a DVR) was made though an equivalent single-phase configuration. In order to filter the high frequency components provided from PWM converter, filtering capacitor and inductors (i.e., passive LCL filter) were connected in parallel with the transformers.

Fig. 10 shows a steady state result in which the MSC is operating as a series-APF. In this case, a 5th harmonic voltage was added with fundamental voltage at the grid (i.e., $v_{ga} = V_g sin(w_g t) + 0.2V_g sin(5w_g t)$). The dc-link voltage ($v_C$) is regulate considering the control strategy described previously. It can be seen that disturbance is well compensated by the converter voltage (v_{ra}). The load voltage waveform (v_{la}) is virtually sinusoidal.

Fig. 11 shows MSC acting as a DVR. The compensator was tested under a voltage sag. It can be seen that the voltage sag is compensated satisfactorily. To guarantee that the injected voltage was in phase with the same angle of the grid, a phase-locked-loop (PLL) based on fictitious electrical power (i.e., power-based PLL) was considered. More details of this PLL are found in [26].

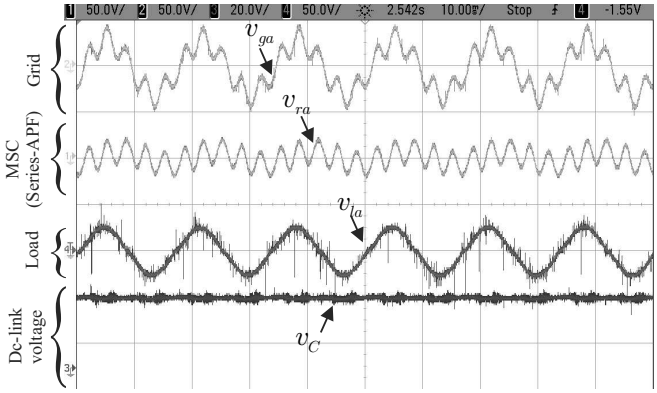

Figure 10. Experimental result. MSC operating as a series-APF. System voltages and the regulated dc-link voltage.

Fig. 12 shows the PWM implementation with proposed MSC having two single-phase transformers per phase (as a consequence it uses converters 1 and 2). In such outcome the transformer turns ratio was considered as $N_1 = 1$ and $N_2 = 2$. Notice that this result is very similar to that one obtained in simulation, see Fig. 8(b). In addition, the converter 2 (with $N_2 = 2$) is clamped most of the time (i.e., it switches 1/3 of the operation cycle) while converter 1 (with $N_1 = 1$) switches over all operation cycle. This is an important characteristic in which the converter 2 will provide lower switching losses in comparison with converter 1. Hence, converter 2 can be implemented with low frequency switches.

Fig. 13, in turn, shows similar result when MSC operates with three single-phase transformers per phase (e.g., using converters 1, 2 and 3). The transformer turns ratios in this result was $N_1 = 1$, $N_2 = 2$ and $N_3 = 4$. As expected the converter 3 (with $N_3 = 4$) provides the lowest switching frequency if compared to converters 2 and 1. The second converter that provide lowest switching is the converter 2 (with $N_2 = 2$). Finally, the converter 1 (with $N_1 = 1$) is the only one that switches over all the time.

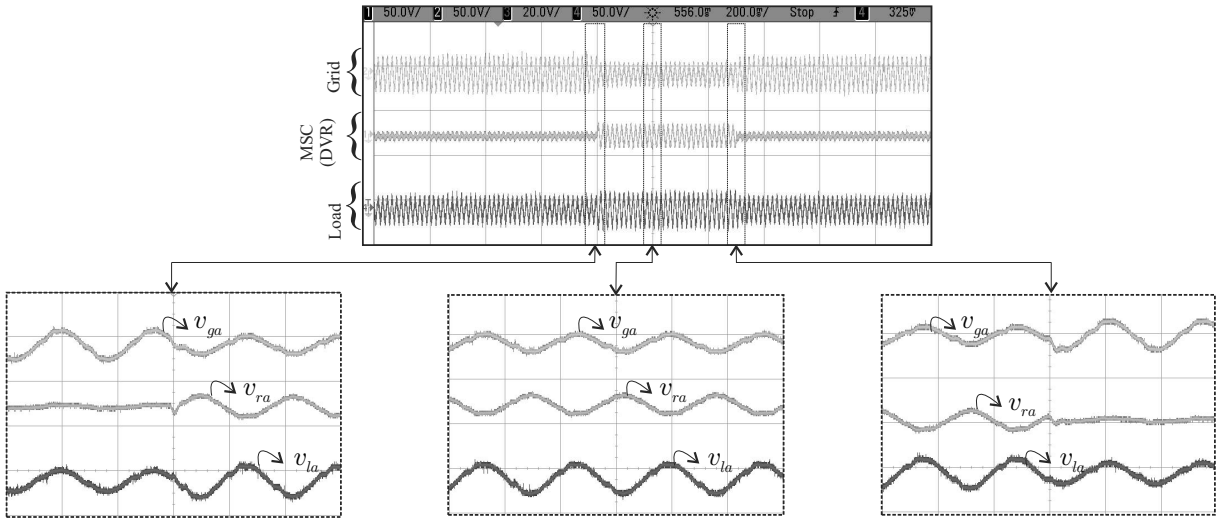

Figure 11. Experimental result. MSC operating as a DVR. System voltages.

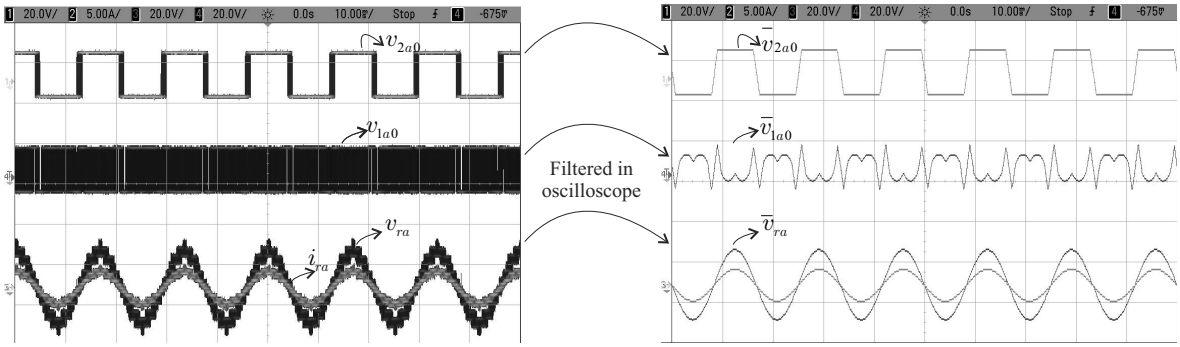

Figure 12. PWM converter voltages in phase a. The PWM implementation of proposed MSC uses two converters (1 and 2) and two transformers per phase with $N_1 = 1$ and $N_2 = 2$.

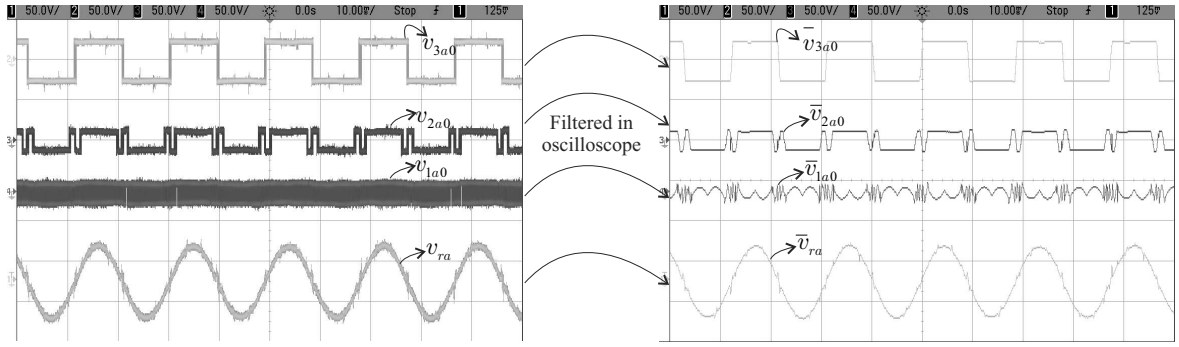

Figure 13. PWM converter voltages in phase a. The PWM implementation of proposed MSC uses three converters (1, 2 and 3) and three transformers per phase with $N_1 = 1$, $N_2 = 2$ and $N_3 = 4$.

XI. Conclusion

This paper has presented a multilevel series compensator (MSC) based on cascaded transformers coupled with three-phase-bridge (TPB) converters. A generalization with K-stages was introduced in order to show that increasing the number of cells the performance is improved as well as increases the power rating of the compensator. The solution is an attractive option due to not need additional dc-link capacitors as observed in some conventional multilevel compensator such as: i) NPC [13], Flying capacitors [15], cascaded HB [16], etc.

Once TPB modules are available in the market, the modularity is fixed as a good feature for this topology. The proposed MSC has two options of operation: (1) as a dynamic voltage restorer (DVR) or (2) as a harmonic series active power

filter (series-APF). Some analyses and comparisons addressing WTHD, semiconductor losses estimation and number of levels generated per power switches were presented. Comparing with conventional HB, the proposed MSC has presented better values for these figures of merit. Simulation and experimental results were presented in order to validate theoretical considerations.

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