Soft-Switching Dual-Flyback DC-DC Converter with Improved Efficiency and Reduced Output Ripple Current

Jae-Won Yang and Hyun-Lark Do

***Abstract*—This paper presents a soft-switching dual-flyback DC-DC converter with improved efficiency and reduced output ripple current. Zero-voltage-switching (ZVS) technique and a dual-flyback module for reducing the number of snubber current paths are adopted to improve efficiency. For ZVS technique, a self-driven synchronous rectifier (SR) is used instead of an output diode. By turning the self-driven SR off after a short delay, a main switch is turned on under the ZVS condition. For reducing the number of snubber current paths, a dual- flyback module and a snubber diode are used. When the main switch is turned off, leakage inductance energy is absorbed by a snubber diode into an input source and a primary DC-bus capacitor. Then, this energy is reprocessed by the dual-flyback DC-DC module to secondary side. Hence, there is only one snubber current path. In addition, the proposed converter features a reduced output ripple current because of the continuous current. Consequently, the proposed converter can achieve high efficiency and reduced output ripple current. To verify the performance of the proposed converter, operating principles, steady-state analyses, and experimental results from a 340 to 24-V, 100-W prototype are presented.**

***Index Terms*—Flyback converter, Zero-voltage-switching, Soft-switching, Synchronous rectifier, Continuous conduction mode.**

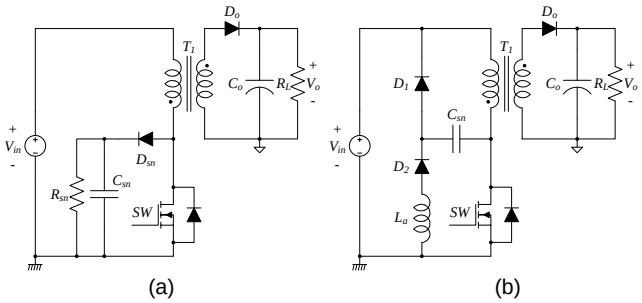


Fig. 1. Conventional flyback DC-DC converter : (a) with a RCD snubber, (b) with a LCD snubber.

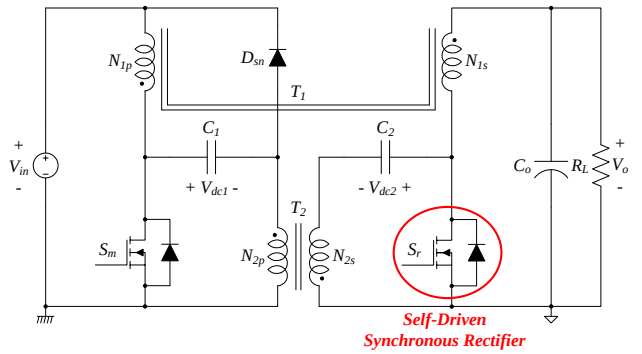


Fig. 2. Proposed converter with self-driven synchronous rectifier.

I. Introduction

FOR the advantages of galvanic isolation, design simplicity, and a simple control technique, a flyback converter is the most popular topology for DC-DC and AC-DC converters [1]-[7]. However, there are some drawbacks such as voltage spike ringing on a switch at turn-off state (because of the resonance between the transformer leakage inductance and the parasitic output capacitance of the switch) and hard switching loss at turn-on state. Eventually, the switch voltage stress becomes as high as the sum of the input voltage, the reflected output voltage, and the voltage spike on the switch. To overcome these problems, two-switch pulse-width modulated (PWM) flyback converters are introduced [4]-[5]. By using two clamping diodes, switch voltage is clamped to input voltage and leakage inductance energy is recycled to input source. In addition, to achieve ZVS turn-on of the switch, an additional lossless snubber circuit is adopted. Another solution for recycling the leakage inductance energy is using an active snubber circuit [6]-[7]. In [6], a half-bridge flyback converter is presented for satisfying both switch voltage clamping and ZVS operation. In [7], an adaptive snubber circuit is introduced to extend the parasitic output capacitance of the switch, and the converter is operated in the critical conduction mode (CRM) for near-ZVS operation. The operation in CRM minimizes the turn-on switching loss of the switch because the MOSFET turn-on occurs exactly in the valley of the drain-source voltage oscillation between a transformer inductor and a parasitic

Manuscript received April 07, 2016; revised July 03, 2016, September 18, 2016 and October 20, 2016; accepted November 29, 2016.

J.-W. Yang is with the 8th research and development institute, Agency for Defense Development, Taean 357-900, Korea (e-mail: fship01@nate.com).

H.-L. Do is with the Department of Electronic and Information Engineering, Seoul National University of Science and Technology, Seoul 139-743, Korea (phone: +82-2-970-6463; fax: +82-2-979-7903; e-mail: hldo@seoultech.ac.kr).

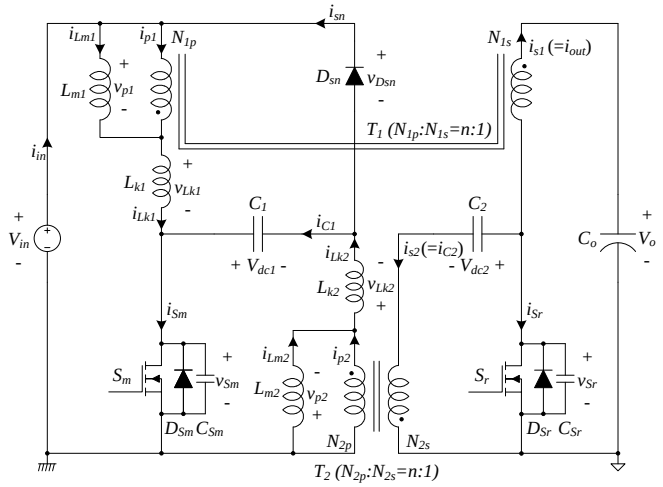


Fig. 3. Equivalent circuit of the proposed converter.

output capacitor of the switch [8]-[10]. Nevertheless, there is a small switching loss in the switch since it is not a full-ZVS operation. Therefore, various soft-switching techniques are introduced for high efficiency [11]-[18]. In addition, a synchronous rectifier (SR) is also introduced instead of a diode for reducing the conduction loss [19]-[23]. Normally, there are three different kinds of *SR* driving strategies—voltage-driving strategy, current-driving strategy [19]-[20], and MOSFET drain-source voltage detection [21]-[23]. By replacing a diode with a *SR*, efficiency is improved because turn-on voltage drop across the *SR* is much lower than diode forward voltage drop.

Fig. 1(a) shows the conventional flyback DC-DC converter with a RCD (resistor-capacitor-diode) snubber. The leakage inductance energy is absorbed by the snubber capacitor and dissipated in the snubber resistor. Fig. 1(b) shows the flyback DC-DC converter with a LCD (inductor-capacitor-diode) snubber. The leakage inductance energy is absorbed by the snubber capacitor and the energy stored in the snubber capacitor is transferred to an auxiliary inductor. This energy is then restored in an input source. Since there are 3 conduction paths (the snubber capacitor, auxiliary inductor, and input source), the reprocessed energy is reduced owing to the conduction loss in a LCD snubber. However, for the proposed converter shown in Fig. 2, the leakage inductance energy is directly stored in an input source and a DC-bus capacitor. Then, this energy is reprocessed by a dual-flyback DC-DC module. Since there is only 1 conduction path, the conduction loss in the reprocessed leakage inductance energy is minimized. When transferring the input power on primary side to secondary side, the input power energy is equally divided between two coupled inductors and transferred to the load because both the coupled inductors are designed to be equal. Hence, the RMS loss in each coupled inductor is reduced. In addition, by turning the self-driven *SR* off after a short delay, a main switch is turned on under the ZVS condition as a result of the differential current via the two coupled inductors. The output ripple current is also lower than that of the conventional flyback DC-DC converter, because of the continuous current in the secondary side. The theoretical analysis and an experimental prototype of the proposed converter are presented to verify the ZVS operation, efficiency improvement, and reduced output ripple current.

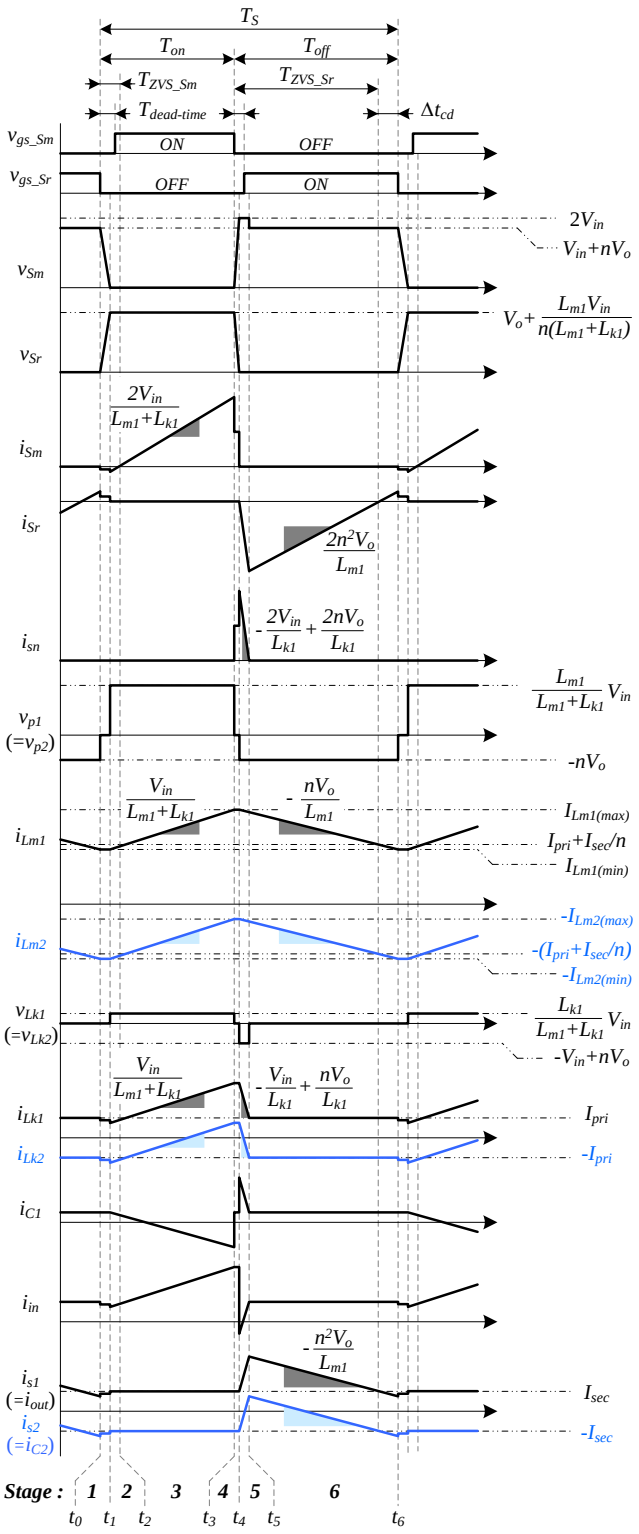


Fig. 4. Theoretical waveforms of the proposed converter.

II. Analysis of the Proposed Converter

Fig. 3 shows the equivalent circuit of the proposed converter. There are three switching devices—a main switch S_m, a synchronous rectifier S_r, and a snubber diode D_{sn}. D_{Sm} and D_{Sr}

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2017.2652404, IEEE Transactions on Industrial Electronics

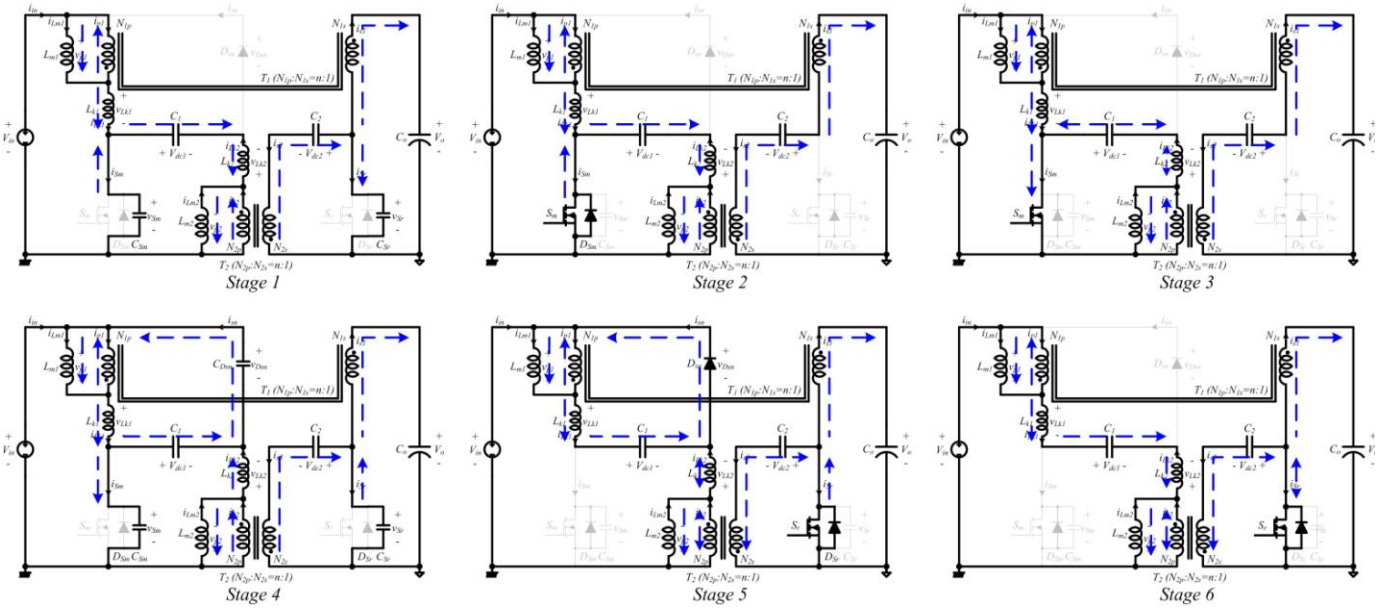


Fig. 5. Operating stages of the proposed converter.

are the intrinsic body diodes of S_m and S_r, respectively. C_{Sm} and C_{Sr} denote the parasitic output capacitances of S_m and S_r, respectively. C_1 and C_2 are the DC-bus capacitors on the primary side and secondary side, respectively. Since input power should be equally divided into two coupled inductors and transferred to load, the coupled inductors should be identical, i.e., T_1=T_2. Each coupled inductor is modeled as a magnetizing inductor L_{m1} (=L_{m2}), a leakage inductor L_{k1} (=L_{k2}), and an ideal transformer with a turn ratio of n:1 (n=N_{1p}/N_{1s}= N_{2p}/N_{2s}). Because the average inductor voltage should be zero at a steady-state, according to the inductor volt-second balance law, V_{dc1} is equal to V_{in} and V_{dc2} is equal to V_o. To analyze the proposed converter at a steady-state, several assumptions are made for a switching period of T_S. All switching devices are ideal components except for C_{Sm} and C_{Sr}. The capacitances of C_1, C_2, and C_o are large enough to consider the voltages V_{dc1}, V_{dc2}, and V_o as constants. The theoretical waveforms over a switching period are shown in Fig. 4. The operating stages are divided into six stages as shown in Fig. 5.

Before t_0, S_r is turned on and its current direction is changed from negative to positive. When the switch current is positive, the absolute value of i_{s2} is larger than that of i_{s1}. This differential current discharges C_{Sm} and charges C_{Sr} at *stage 1*. On the primary side, there is a continuous current I_{pri} for V_{dc1} to become equal to V_{in} because V_{dc1} is slightly lower than V_{in}. On the secondary side also, there is a continuous current I_{sec} for V_{dc2} to become equal to V_o because V_{dc2} is slightly higher than V_o.

Stage 1 [t_0, t_1]: When S_r is turned off, C_{Sm} starts discharging and C_{Sr} begins charging. Since C_{Sm} and C_{Sr} are very small, the transition time is very short. Hence, i_{Lm1} and i_{Lm2} are regarded as constant values— $I_{Lm1(min)}$ and -$I_{Lm2(min)}$, respectively.

Stage 2 [t_1, t_2]: At t_1, C_{Sm} is fully discharged and D_{Sm} starts conducting because the absolute value of i_{Lk2} is larger than that of i_{Lk1}. After a short delay called a dead-time, the gate signal is applied to S_m under the ZVS condition. Therefore, there is no switching loss on S_m. At this stage, the slopes of i_{Lm1}, i_{Lk1}, i_{Lm2}, and i_{Lk2} are all equal to $V_{in}/(L_{m1}+L_{k1})$.

$$i_{Lm1}(t) = I_{Lm1(\min)} + \frac{V_{in}}{L_{m1}+L_{k1}}(t-t_1), \tag{1}$$

$$i_{Lm2}(t) = -I_{Lm2(\min)} + \frac{V_{in}}{L_{m1}+L_{k1}}(t-t_1). \tag{2}$$

At the secondary side, I_{sec} flows through two secondary windings of the coupled inductors. The currents i_{s1} and i_{s2} are constants (I_{sec} and -I_{sec}, respectively).

Stage 3 [t_2, t_3]: When the main switch current i_{Sm} becomes positive, this stage begins. Similar to *stage 2*, the slopes of i_{Lm1}, i_{Lk1}, i_{Lm2}, and i_{Lk2} are all equal to $V_{in}/(L_{m1}+L_{k1})$. At t_2, $i_{Lk1}(t_2)$ and $i_{Lk2}(t_2)$ are equal to I_{pri} and -I_{pri}, respectively.

$$i_{Lk1}(t) = I_{pri} + \frac{V_{in}}{L_{m1}+L_{k1}}(t-t_2), \tag{3}$$

$$i_{Lk2}(t) = -I_{pri} + \frac{V_{in}}{L_{m1}+L_{k1}}(t-t_2). \tag{4}$$

i_{Lm1} and i_{Lm2} increase linearly from I_{pri}+I_{sec}/n and -(I_{pri}+I_{sec}/n).

$$i_{Lm1}(t) = I_{pri} + \frac{I_{\sec}}{n} + \frac{V_{in}}{L_{m1}+L_{k1}}(t-t_2), \tag{5}$$

$$i_{Lm2}(t) = -I_{pri} - \frac{I_{\sec}}{n} + \frac{V_{in}}{L_{m1}+L_{k1}}(t-t_2). \tag{6}$$

At the middle of this stage, i_{Lk2} changes its direction from negative to positive since the absolute value of i_{Lm2} is smaller than i_{p2} (=-i_{s2}/n=I_{sec}/n).

Stage 4 [t_3, t_4]: At t_3, S_m is turned off. C_{Sm} starts charging and C_{Dsn} and C_{Sr} begin to discharge. At this stage, the capacitor C_{Dsn} (which is the parasitic capacitor of the snubber diode D_{sn}) is considered because the leakage current flows through D_{sn}.

However, since C_{Sm}, C_{Dsn}, and C_{Sr} are very small, the transition time is very short. Hence, i_{Lm1} and i_{Lm2} can be regarded as constant values— $I_{Lm1(max)}$ and $-I_{Lm2(max)}$, respectively.

Stage 5 [t_4, t_5]: When v_{Sm} reaches $2V_{in}$, D_{sn} and D_{Sr} start conducting. The leakage inductance energy of L_{k1} is stored into C_1. For L_{k2}, the leakage inductance energy is stored into the input source. This time interval is closely related to the voltage v_{Lk1} ($=v_{Lk2}$). i_{Lk1} and i_{Lk2} are expressed as given below:

$$i_{Lk1}(t) = I_{Lk1(\max)} - \frac{1}{L_{k1}}(V_{in} - nV_o)(t - t_4), \tag{7}$$

$$i_{Lk2}(t) = I_{Lk2(\max)} - \frac{1}{L_{k2}}(V_{in} - nV_o)(t - t_4). \tag{8}$$

Stage 6 [t_5, t_6]: When i_{Dsn} is zero and D_{sn} is turned off, this stage begins. On the primary side, only I_{pri} flows through L_{k1}, C_1, and L_{k2}. After a short delay called a dead-time, the gate signal is applied to S_r under the ZVS condition. The current i_{Sr} increases linearly with a slope of $2n^2V_o/L_{m1}$. At the end of this stage, i_{Sr} changes its direction from negative to positive. By turning the *SR* off after a short delay, the absolute value of i_{s2} becomes larger than that of i_{s1}. This differential current is essential for the ZVS operation of S_m.

III. Analysis of the Self-driven *SR* Circuit

The self-driven *SR* driver used in this paper is referenced from [22]. Fig. 6 shows the self-driven *SR* driver. C_{ceo} is the parasitic output capacitor of Q_a. In order to detect the polarity of the *SR* voltage v_{Sr}, D_a is employed. To obtain high and low signals according to the polarity of v_{Sr}, a NPN transistor Q_a and two resistors, R_b and R_c, are used. R_b limits the base current i_{Rb} of Q_a. R_c is inserted to limit the collector current i_{Rc}, and to generate high-level signal for the MOSFET driver with a dead-time. For the proper ZVS operation of S_r, the dead-time should be considered and it is related to the time constant of the *RC* circuit, V_{cc}, R_c, and C_{ceo}. To compensate for the difference between the forward voltage drop $V_{F(Da)}$ and the base-emitter saturation voltage $V_{be(sat)}$, R_a is added. Several assumptions are made in the analysis at a steady state. D_a is an ideal component, except for the forward voltage drop $V_{F(Da)}$. Q_a acts as a switch, and not as a signal amplifier. The base-emitter input capacitor is not considered. The *SR* is an ideal component, except for the drain-source on-resistance $R_{DS(on)}$ and the forward voltage drop $V_{F(Dsr)}$. The theoretical waveforms and operating stages of the self-driven *SR* driver are shown in Figs. 7 and 8.

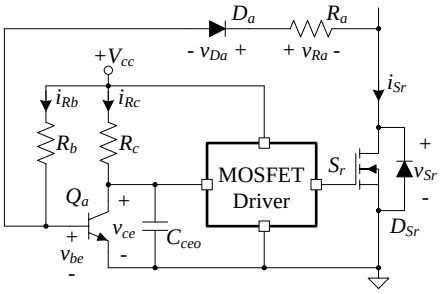


Fig. 6. Self-driven synchronous rectifier driver.

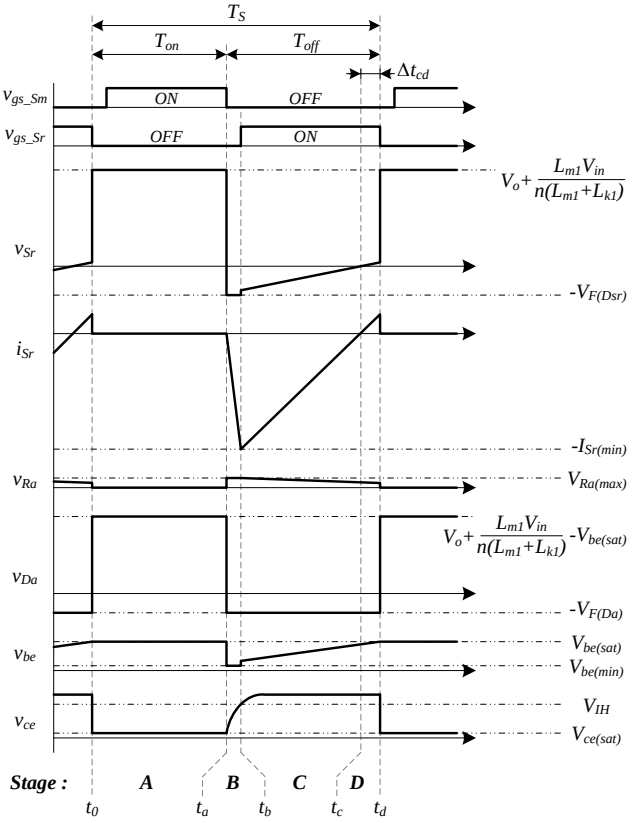


Fig. 7. Theoretical waveforms of the proposed SR driver.

Before t_0, S_r is turned on and D_a conducts. The base-emitter voltage v_{be} is lower than its saturation voltage $v_{be(sat)}$.

Stage A [t_0, t_a]: When v_{be} reaches $v_{be(sat)}$, Q_a becomes saturated and this stage begins. The collector-emitter voltage v_{ce} is clamped to its saturation voltage $v_{ce(sat)}$, and S_r is turned off.

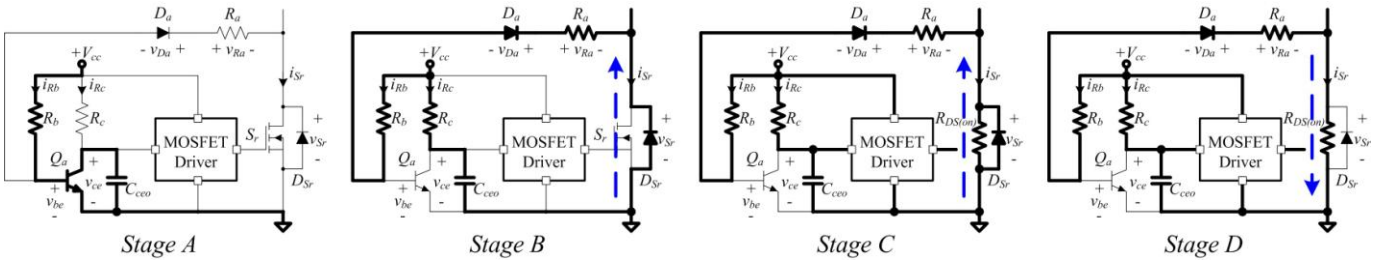


Fig. 8. Operating stages of the proposed SR driver.

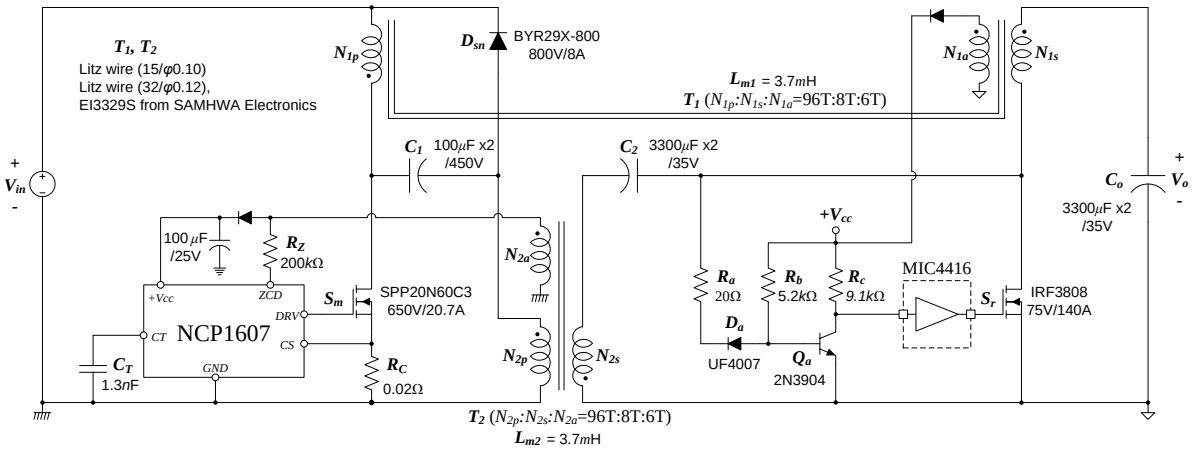


Fig. 9. Experimental prototype circuit of the proposed converter.

Stage B [t_a, t_b]: At t_a, S_m is turned off. D_{Sr} and D_a start conducting. v_{Sr} and v_{Da} are clamped to the forward voltage drops, $-V_{F(Dsr)}$ and $-V_{F(Da)}$, respectively. Since v_{Sr} and v_{Da} are constant, v_{be} and v_{Ra} are also constant as given below:

$$v_{be(\min)} = V_{F(Da)} + V_{Ra(\max)} - V_{F(Dsr)}, \tag{9}$$

$$V_{Ra(\max)} = \frac{R_a(V_{cc} - V_{be(\min)})}{R_b}. \tag{10}$$

Because v_{be} is lower than $V_{be(sat)}$, Q_a enters a breakdown region. v_{ce} increases nonlinearly with the time constant of a *RC* circuit as follows:

$$v_{ce}(t) = V_{cc}\left(1 - e^{\frac{-t}{R_c C_{ceo}}}\right). \tag{11}$$

Stage C [t_b, t_c]: When v_{ce} is higher than V_{IH}, which is the logic 1 input voltage of the MOSFET driver, the gate signal v_{gs_Sr} is applied to S_r. In this stage, S_r is expressed as a parallel circuit of $R_{DS(on)}$ and D_{Sr}. The voltage v_{be} is expressed as given below:

$$v_{be}(t) = V_{F(Da)} + R_a i_{Rb}(t) + R_{DS(on)} i_{Sr}(t), \tag{12}$$

$$i_{Rb}(t) = \frac{V_{cc} - v_{be}(t)}{R_b}, \tag{13}$$

$$i_{Sr}(t) = -I_{Sr(\min)} + \frac{2n^2 V_o}{L_{m1}}(t - t_b). \tag{14}$$

Stage D [t_c, t_d]: At t_c, i_{Sr} changes its direction from negative to positive. Since v_{be} is still lower than $V_{be(sat)}$, S_r is turned on.

$$v_{be}(t) = V_{F(Da)} + R_a i_{Rb}(t) + R_{DS(on)} \frac{2n^2 V_o}{L_{m1}}(t - t_c). \tag{15}$$

To compensate for the difference between $V_{F(Da)}$ and $V_{be(sat)}$, R_a is added in series with D_a. By adjusting R_a, the turn-on time of S_r can be easily controlled. At the end of this stage, v_{be} reaches $v_{be(sat)}$, and then S_r is turned off. $v_{be(sat)}$ is obtained by

$$v_{be(sat)} = V_{F(Da)} + R_a i_{Rb}(t_d) + R_{DS(on)} \frac{2n^2 V_o}{L_{m1}} \Delta t_{cd}, \tag{16}$$

$$i_{Rb}(t_d) = \frac{V_{cc} - v_{be(sat)}}{R_b}, \tag{17}$$

where, Δt_{cd} is the time interval between t_c and t_d.

From (16) and (17), Δt_{cd} can be expressed as

$$\Delta t_{cd} = \left(\frac{R_a + R_b}{R_b} V_{be(sat)} - V_{F(Da)} - \frac{R_a}{R_b} V_{cc}\right) \times \frac{L_{m1}}{2n^2 V_o R_{DS(on)}}. \tag{18}$$

Hence, it is possible to control the time interval Δt_{cd} (related to the ZVS operation of S_m) by adjusting the resistance of R_a.

IV. ZVS Condition of the Main Switch

In order to achieve ZVS operations for S_m and S_r, the gate signal should be applied to each switch before the current flowing through the intrinsic body diode becomes zero. The following equations are satisfactory conditions for the ZVS operations of S_m and S_r as shown in Fig. 4.

$$T_{dead-time} < T_{ZVS\_Sm}, \tag{19}$$

$$T_{dead-time} < T_{ZVS\_Sr}, \tag{20}$$

where, $T_{dead\text{-}time}$ is the dead-time of both S_m and S_r for proper ZVS operation. T_{ZVS_Sm} and T_{ZVS_Sr} are the time intervals when each switch is reverse-biased and the current flows through its intrinsic body diode.

Since T_{ZVS_Sr} is sufficiently longer than $T_{dead\text{-}time}$, the ZVS operation of S_r is always satisfactory. When considering $T_{dead\text{-}time}$ and T_{ZVS_Sm}, the time interval between t_0 and t_1 can be omitted because this time interval is very short. From i_{Lm1} in Fig. 4, the following equation is obtained.

$$I_{pri} + \frac{I_{\sec}}{n} - I_{Lm1(\min)} = \frac{V_{in}}{L_{m1} + L_{k1}} T_{ZVS\_Sm} = \frac{nV_o}{L_{m1}} \Delta t_{cd}. \tag{21}$$

From (19) and (21), the ZVS condition of S_m can be rewritten.

$$T_{dead-time} < \frac{nV_o(L_{m1} + L_{k1})}{V_{in} L_{m1}} \Delta t_{cd}. \tag{22}$$

V. Design Procedure

In order to verify the theoretical analysis, the following design specifications are determined. V_{in}=340V, V_o=24V, P_o=100W, and minimum switching frequency $f_{SW(\min)}$= 45kHz. For a simple circuit analysis, the leakage inductances and the transition times in both *stages 1* and *4* are not considered.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2017.2652404, IEEE Transactions on Industrial Electronics

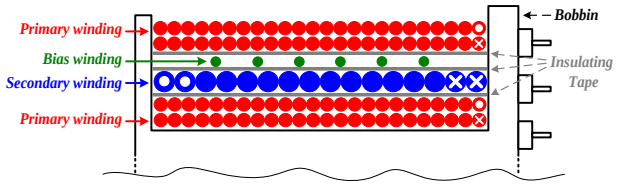


Fig. 10. Structure of the coupled inductor.

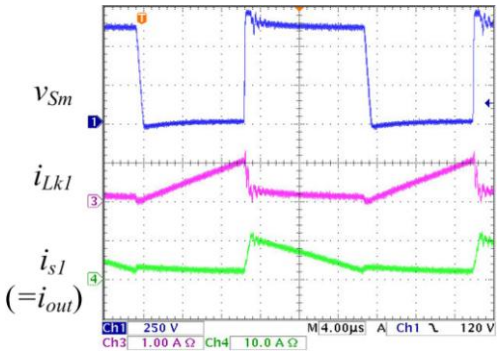
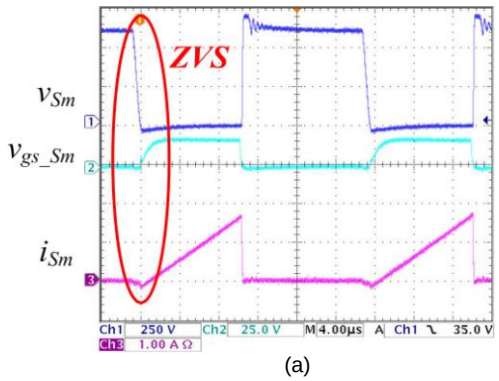
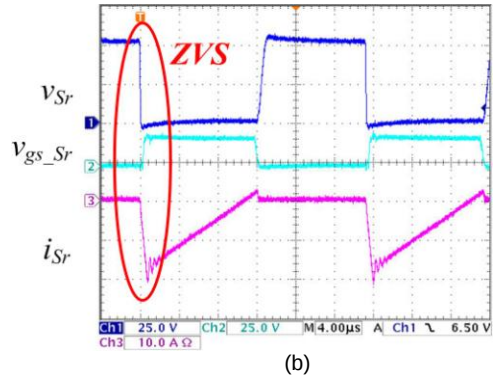


Fig. 11. Experimental waveforms of v_{Sm}, i_{Lk1}, i_{s1}(=i_{out}) at P_o=100W.



(a)



(b)

Fig. 12. ZVS operations of S_m and S_r at 100W: (a) v_{Sm}, v_{gs_Sm}, i_{Sm}, (b) v_{Sr}, v_{gs_Sr}, i_{Sr}.

A. Duty cycle

From i_{Lm1}, the following equation is obtained.

$$I_{Lm1(\max)} - I_{Lm1(\min)} = \frac{V_{in}}{L_{m1}} T_{on} = \frac{nV_o}{L_{m1}} T_{off} . \quad (23)$$

From (23), the duty cycle D is expressed as:

$$D = \frac{nV_o}{V_{in} + nV_o} . \quad (24)$$

B. Continuous current

By assuming the leakage inductance to be zero, the average input and output currents in a switching period are given by

$$I_{in(avg)} = I_{pri} + \frac{V_{in}}{2L_{m1}} D^2 T_S , \quad (25)$$

$$I_{out(avg)} = I_{\sec} + \frac{n^2 V_o}{2L_{m1}} (1-D)^2 T_S . \quad (26)$$

Since the snubber current is not considered, the input current is the sum of the continuous current for charging C_1 and the charging current flowing through L_{m1}. Because the magnetizing inductances of both the coupled inductors are designed to be equal, one half of the input power is transferred to the secondary side by L_{m1} and the other half is transferred by L_{m2}. Therefore, I_{pri} is half of the input current, I_{pri}=0.5$I_{in(avg)}$.

Similarly, the output current is the sum of the continuous current for discharging C_2 and the discharging current flowing through L_{m2}. Since one half of the output power is transferred from the primary side by L_{m1} and the other half is transferred by L_{m2}, I_{sec} is also half of the output current, I_{sec}=0.5$I_{out(avg)}$.

C. Design of coupled inductors

The determination of the turn ratio n is important for transferring the input power to the load. When the main switch is turned off and the primary voltage of the coupled inductor nV_o is lower than V_{in}, the magnetizing inductance energy is transferred to the secondary side. However, if the primary voltage is higher than the input voltage, the coupled inductor acts only as an inductor, and not as a transformer. Therefore, the maximum turn ratio n is determined by

$$n < \frac{V_{in}}{V_o} . \quad (27)$$

By substituting I_{pri}=0.5$I_{in(avg)}$ in (25), L_{m1} can be obtained by

$$L_{m1} = \frac{V_{in} D^2 T_S}{I_{in(avg)}} . \quad (28)$$

If n=12 is selected, D=0.45 is obtained. By substituting V_{in}=340 V, D=0.45, T_S=22µsec, and $I_{in(avg)}$=0.294A in (28), L_{m1}=5.1mH is calculated. Since the leakage inductance is not considered in the design procedure, the experimental value of L_{m1}(=L_{m2}) would be different. The reason is that some of the magnetizing inductance energy is not transferred to the secondary side. This energy is moved to the input source and the primary DC-bus capacitor by each leakage inductor.

D. Determination of switching frequency

The input current can be expressed as an average current of i_{Sm} as follows:

$$I_{in} = i_{Sm(avg)} = \frac{V_{in}}{L_{m1} + L_{k1}} D^2 T_S . \quad (29)$$

By substituting T_S=1/f_{sw} and $V_{in}I_{in}$=P_{in}=P_{out} in (29), the switching frequency f_{sw} can be written as below

$$f_{sw} = \frac{V_{in}^2}{P_o (L_{m1} + L_{k1})} \left(\frac{nV_o}{V_{in} + nV_o} \right)^2 . \quad (30)$$

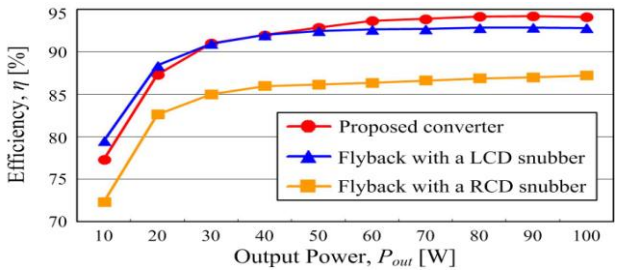


Fig. 13. Measured efficiencies of the proposed and conventional converters.

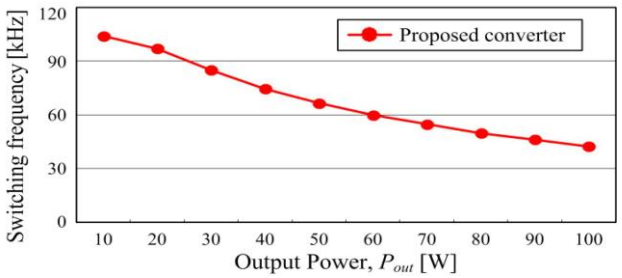


Fig. 14. Measured switching frequency of the proposed converter.

VI. Experimental Results

From the design procedure, the design parameters of the experimental prototype are obtained as follows: L_{m1}=L_{m2}=3.7 mH, n=12, C_1=200μF, C_2=6.6mF, and C_o=6.6mF. Fig. 9 shows the experimental prototype circuit. Fig. 10 shows the structure of the coupled inductor.

Fig. 11 shows the experimental waveforms of v_{SW}, i_{Lk1}, and i_{s1} (=i_{out}) at P_o=100W. Since half of the input power is transferred to C_1, the leakage inductor current is floating because of the continuous current. Similarly, the output current is also floating since half of the output power is stored in C_2 and is transferred to the output capacitor by the continuous current.

Figs. 12(a) and (b) show the ZVS operations of S_m and S_r at 100W, respectively. Before the gate signal is applied to each switch, the switch voltage is zero.

Fig. 13 shows the measured efficiencies of the proposed converter and the conventional flyback converters with RCD and LCD snubbers shown in Figs. 1(a) and (b). The controller power consumption is included. For a fair comparison, the conventional flyback converters are designed with the same design specifications and operated in CRM. For the RCD and LCD snubbers, R_{sn}=320kΩ and L_a=20.9mH are used. It is clear that the proposed converter is the most efficient converter among them for medium and heavy loads. The reason is that the leakage inductance energy is directly stored in an input source and a primary DC-bus capacitor equally. Then, this energy is reprocessed by a dual-flyback DC-DC module. The maximum efficiency of the proposed converter η_{max}=94.18% is measured at P_o=90W. However, at a light load, the proposed converter features lower efficiency than the conventional flyback converter with the LCD snubber. This is because the reverse current for achieving ZVS operation increases the conduction losses on both the switches and the coupled inductors. Fig. 14 shows the measured switching frequency according to the output power. At the full-load condition, a switching frequency (f_{sw}) of 42.3kHz has been measured.

VII. Conclusion

In this paper, a soft-switching dual-flyback DC-DC converter was proposed. By replacing the output diode with an *SR*, the conduction loss was minimized. The ZVS operation of the main switch was achieved by turning the self-driven *SR* off, after a short delay. In addition, the reprocessed transformer leakage inductance energy was maximized because there was only one snubber current path. Moreover, its output ripple current was reduced owing to the continuous current. Consequently, the proposed converter satisfied both the high efficiency and reduced output ripple current conditions.

References

[1] J.-W. Kim, J.-P. Moon and G.-W. Moon, "Analysis and Design of a Single-Switch Forward-Flyback Two-Channel LED Driver With Resonant-Blocking Capacitor," *IEEE Trans. Power Electron.*, vol. 31, DOI 10.1109/TPEL.2015.2432458, no. 3, pp. 2314-2323, Mar. 2016.

[2] Y. Chen, C. Chang and P. Yang, "A Novel Primary-Side Controlled universal-Input AC-DC LED Driver Based on a Source-Driving Control Scheme," *IEEE Trans. Power Electron.*, vol. 30, DOI 10.1109/TPEL.2014.2359585, no. 8, pp. 4327-4335, Aug. 2015.

[3] J.-W. Shin, S.-J. Choi and B.-H. Cho, "High-Efficiency Bridgeless Flyback Rectifier With Bidirectional Switch and Dual Output Windings," *IEEE Trans. Power Electron.*, vol. 29, DOI 10.1109/TPEL.2013.2283073, no. 9, pp. 4752-4762, Sep. 2014.

[4] K. Soltanzadeh, H. Khalilian and M. Dehghani, "Analysis, design and implementation of a zero voltage switching two-switch CCM flyback converter," *IET Circuits, D. & S.*, vol. 10, DOI 10.1049/iet-cds.2014.0329, Iss. 1, pp. 20-28, Jan. 2016.

[5] M. Mohammadi and E. Adib, "Lossless passive snubber for half bridge interleaved flyback converter," *IET Power Electron.*, vol. 7, DOI 10.1049/iet-pel.2013.0394, Iss. 6, pp. 1475-1481, June 2014.

[6] J.-K. Kim, J.-B. Lee and G.-W. Moon, "Zero-Voltage Switching Multioutput Flyback Converter With Integrated Auxiliary Buck Converter," *IEEE Trans. Power Electron.*, vol. 29, DOI 10.1109/TPEL.2013.2276443, no. 6, pp. 3001- 3010, June 2014.

[7] M. A. Rezaei, K.-J. Lee and A. Q. Huang, "A High-Efficiency Flyback Micro-inverter With a New Adaptive Snubber for Photovoltaic Applications," *IEEE Trans. Power Electron.*, vol. 31, DOI 10.1109/TPEL.2015.2407405, no. 1, pp. 318-327, Jan. 2016.

[8] T. Yan, J. Xu, F. Zhang, J. Sha and Z. Dong, "Variable-On-Time-Controlled Critical-Conduction-Mode Flyback PFC Converter," *IEEE Trans. Ind. Electron.*, vol. 61, DOI 10.1109/TIE.2014.2311401, no. 11, pp. 6091-6099, Nov. 2014.

[9] X. Xie, C. Zhao, L. Zheng and S. Liu, "An Improved Buck PFC Converter With High Power Factor," *IEEE Trans. Power Electron.*, vol. 28, DOI 10.1109/TPEL.2012.2214060 , no. 5, pp. 2277-2284, May 2013.

[10] X. Wu, J. Yang, J. Zhang and Z. Qian, "Variable On-Time (VOT)-Controlled Critical Conduction Mode Buck PFC Converter for High-Input AC/DC HB-LED Lighting Applications," *IEEE Trans. Power Electron.*, vol. 27, DOI 10.1109/TPEL.2011.2169812, no. 11, pp. 4530-4539, Nov. 2012.

[11] C.-H. Chang, C.-A. Cheng, E.-C. Chang, H.-L. Cheng and B.-E. Yang, "An Integrated High-Power-Factor Converter With ZVS Transition," *IEEE Trans. Power Electron.*, vol. 31, DOI 10.1109/TPEL.2015.2439963, no.3, pp. 2362-2371, Mar. 2016.

[12] X. Huang, F. C. Lee, Q. Li and W. Du, "High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor," *IEEE Trans. Power Electron.*, vol. 31, DOI 10.1109/TPEL.2015.2476482, no. 6, pp. 4343-4352, June 2016.

[13] Y. Shi and X. Yang, "Soft Switching PWM Cascaded Three-Level Combined DC-DC Converters With Reduced Filter Size and Wide ZVS Load Range," *IEEE Trans. Power Electron.*, vol. 30, DOI 10.1109/TPEL.2015.2391285, no. 12, pp. 6604-6616, Dec. 2015.

[14] S. Sathyan, H. M. Suryawanshi, M. S. Ballal and A. B. Shitole, "Soft-Switching DC-DC Converter for Distributed Energy Sources With High Step-Up Voltage Capability," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2015.2448515, no. 11, pp. 7039-7050, Nov. 2015.

[15] L. Chen, C. Hu, Q. Zhang, K. Zhang and I. Batarseh, "Modeling and Triple-Loop Control of ZVS Grid-Connected DC/AC Converters for Three-Phase Balanced Microinverter Application," *IEEE Trans. Power Electron.*, vol. 30, DOI 10.1109/TPEL.2014.2329278, no. 4, pp. 2010-2023, Apr. 2015.

[16] O. Husev, L. Liivik, F. Blaabjerg, A. Chub, D. Vinnikov and I. Roasto, "Galvanically Isolated Quasi-Z-Source DC-DC Converter With a Novel ZVS and ZCS Technique," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2015.2455522, no. 12, pp. 7547-7556, Dec. 2015.

[17] M. R. Mohammadi and H. Farzanehfard, "Analysis of Diode Reverse Recovery Effect on the Improvement of Soft-Switching Range in Zero-Voltage-Transition Bidirectional Converters," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2014.2363425, no. 3, pp. 1471-1479, Mar. 2015.

[18] W.-J. Cha, Y.-W. Cho, J.-M. Kwon and B.-H. Kwon, "Highly Efficient Microinverter With Soft-Switching Step-Up Converter and Single-Switch-Modulation Inverter," *IEEE Trans. Ind. Electron.*, vol. 62, DOI 10.1109/TIE.2014.2366718, no. 6, pp. 3516-3523, June 2015.

[19] J. Zhang, J. Wang, G. Zhang and Z. Qian, "A Hybrid Driving Scheme for Full-Bridge Synchronous Rectifier in LLC Resonant Converter," *IEEE Trans. Power Electron.*, vol. 27, DOI 10.1109/TPEL.2011.2180027, no. 11, pp. 4549-4561, Nov. 2012.

[20] J. Zhang, J. Liao, J. Wang and Z. Qian, "A Current-Driving Synchronous Rectifier for an LLC Resonant Converter With Voltage-Doubler Rectifier Structure," *IEEE Trans. Power Electron.*, vol. 27, DOI 10.1109/TPEL.2011.2167520, no. 4, pp. 1894- 1904, Apr. 2012.

[21] E. Mujjalinvimut, P. N. N. Ayudhya and A. Sangswang, "An Improved Asymmetrical Half-Bridge Converter With Self-Driven Synchronous Rectifier for Dimmable LED Lighting," *IEEE Trans. Ind. Electron.*, vol. 63, DOI 10.1109/TIE.2015.2477263, no. 2, pp. 913-925, Feb. 2016.

[22] J.-W. Yang and H.-L. Do, "High-Efficiency ZVS AC-DC LED Driver Using a Self-Driven Synchronous Rectifier," *IEEE Trans. Circuits and Systems-I*, DOI 10.1109/TCSI.2014.2309837, vol. 61, DOI 10.1109/TCSI.2014.2309837, no. 8, pp. 2505-2512, Aug. 2014.

[23] J. Park, Y.-S. Roh, Y.-J. Moon and C. Yoo, "A CCM/DCM Dual-Mode Synchronous Rectification Controller for a High-Efficiency Flyback Converter," *IEEE Trans. Power Electron.*, vol. 29, DOI 10.1109/TPEL.2013.2256371, no. 2, pp. 768-774, Feb. 2014.

Jae-Won Yang received the B.S. and M.S. degrees in electronic and information engineering from Seoul National University of Science and Technology, Seoul, Korea, in 2011 and 2014, respectively.

From 2014, he has been a Researcher with the 8th Research and Development Institute, Agency for Defense Development, Taean, Korea. His research interests include power factor correction, dc-dc power converter, renewable energy conversion, and LED lighting.

Hyun-Lark Do received the B.S. degree from Hanyang University, Seoul, Korea, in 1999, and the M.S. and Ph.D. degrees in electronic and electrical engineering from the Pohang University of Science and Technology, Pohang, Korea, in 2002 and 2005, respectively.

From 2005 to 2008, he was a Senior Research Engineer with the PDP Research Laboratory, LG Electronics Inc., Gumi, Korea. Since 2008, he has been with the Department of Electronic and Information Engineering, Seoul National University of Science and Technology, Seoul, Korea, where he is currently a Professor. His research interests include the modeling, design and control of power converters, soft-switching power converters, resonant converters, PFC circuits, and driving circuits for plasma display panels.