A Novel Switched-capacitor Multilevel Inverter Offering Modularity in Design

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***Abstract*—A new topology of switched-capacitor (SC) multilevel inverter (MLI) which enables modular design is presented in this paper. By employing the series-parallel SC technique, the proposed MLI provides voltage step-up capability and self-balancing of the capacitor voltage. Since the maximum voltage stress of the capacitors and the switches is limited by the proposed topology and independent of the number of output voltage levels, the SCMLI can be modularized with low-voltage SC units to form a scalable inverter with substantial decrease in production cost. In this paper, the key features and operation principle of the proposed topology are described. The capacitor voltage ripples and the associated energy loss of the SCMLI with staircase modulation under different loading conditions and operating frequencies are analyzed and the consideration for component sizing is discussed. The operation of the proposed topology is verified by the simulation and experiment on a 9-level SCMLI with three SC units.**

Keywords—multi-level inverter, series-parallel conversion, switched-capacitor circuit

I. INTRODUCTION

Multilevel voltage-source inverters offer many superior features over the two-level counterparts. These features include the improvement of output voltage quality and the performance in electromagnetic interference, as well as the reduction in the voltage stress and *dv/dt* stresses of components which allows medium-to-high voltage output without the necessity of step-up transformers. However, the shortcomings including the capacitor voltage balancing issues and the requirement of isolated DC sources limit the number of output levels and the applications of the conventional multilevel inverters (MLIs) such as the flying capacitor (FC), neutral point clamped (NPC) and cascaded H-bridge (CHB) inverters [1-4]. The MLIs based on series-parallel switched-capacitor (SC) technique have gained increasing attention in recent years since they eliminate the need of independent voltage sources [5-6], allow capacitor voltage balancing [5-10], and reduce the converter complexity [6-11]. However, most of the existing topologies have limited system modularity due to the dramatic increase in voltage stress of the semiconductor switches with the growing numbers of SC units and output voltage levels. Although employing a single H-bridge back-end for generating bipolar output voltage could substantially save the component count, this negates the benefit of component rating reduction offered by the MLIs [12].

Instead of an H-bridge back-end, the proposed topology employs a novel bipolar series-parallel conversion technique to produce bipolar voltage output. The concept of cross-switched structure [13-15] and the series-parallel SC technique are adopted in the topology to step-up the voltage with an H-bridge front-end. Self-voltage balancing [6] of the capacitors is achieved by the parallel operation, which refresh the capacitor voltage at twice of the fundamental frequency. Since the voltage stress of the components are limited by the DC source voltage and the topology, which is independent of the number of SC units and output voltage levels, the proposed SCMLI has high degree of modularity.

In this paper, the technical description on the structure of the proposed SCMLI as well as the operation principle are provided. The switching sequence for generating different output voltage levels and refreshing the voltages of capacitors are explained. The mathematical analyses on the effects of operating frequency and output current to the capacitor voltage ripples and charge-up power losses of the inverter under staircase modulation technique are also included. The operation of the proposed topology is verified by the simulation and experiment of the MLIs with three SC units. The simulated and measured waveforms, showing the gate signals, output voltage and current, as well as the capacitor voltage are presented in later section.

II. PROPOSED SCMLI TOPOLOGY

The proposed SCMLI utilizes the bipolar series-parallel SC technique to charge the capacitors and boost the voltage in forward and reverse directions. In this section, the structure and the working principle of the proposed SCMLI are described.

A. Overview of the Proposed SCMLI

The proposed SCMLI consists of – 1) a triple-half-bridge front-end connecting to the DC voltage source, 2) SC units, and 3) a half-bridge back-end connecting to the last SC unit and the load. The generalized structure of the proposed topology is illustrated in Fig. 1. Each of the SC units consists of three switches and a capacitor to provide two additional output voltage levels. Combining with the triple-half-bridge front-end and the half-bridge back-end, a SCMLI with k SC units is capable of generating $2k+3$ output levels and an output voltage range of $\pm(k+1)V_s$. The key parameters of a k-unit

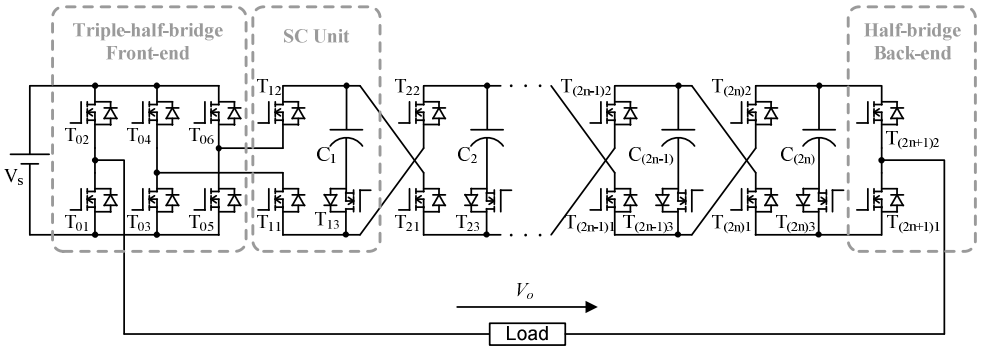

Fig. 1. Generalized structure of the proposed SCMLI; a 4n+3-level MLI consists of 2n SC units

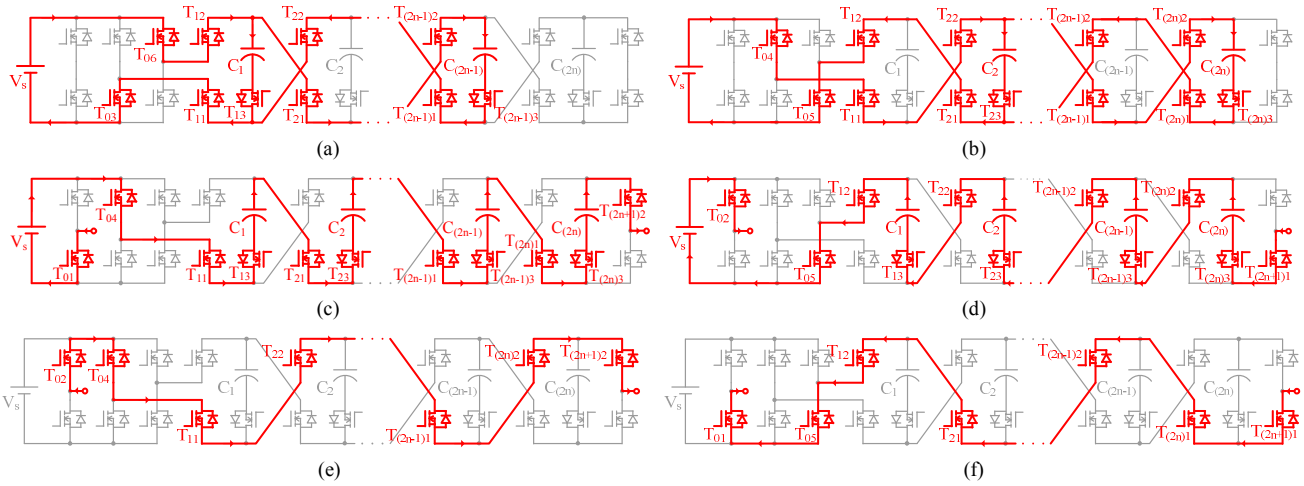

Fig. 2. Operations of the SC units; (a) parallel operation for charging odd SC units; (b) parallel operation for charging the even SC units; (c) series operation for the positive peak output voltage; (d) series operation for the negative peak output voltage; (e) and (f) by-pass the SC units

SCMLI employing the proposed topology are summarized in table I.

In this presented topology, regardless of the number of SC units, the voltage across the input and output terminals of each SC unit is limited to $\pm V_s$, which bounds the voltage stress of the semiconductor switches to $2V_s$; and the stress of the half-bridges is only one V_s. Therefore, a high voltage MLI can be constructed with low voltage DC source, several low voltage SC modules and half-bridges.

TABLE I. KEY PARAMETERS OF THE PROPOSED SCMLI TOPOLOGY

Parameter	Value
No. of switched-capacitors	k
No. of output levels	$2k$+3
No. of switches	$3k$+8
Switched-capacitor voltage	V_s
Maximum output voltage	$(k+1)V_s$
Voltage stress of switches (T_{01} to T_{06}, $T_{(k+1)1}$ and $T_{(k+1)2}$)	V_s
Voltage stress of switches (T_{11} to T_{k3})	$2V_s$

B. *Description of the SC Operations*

The H-bridge front-end and the SC units form the bipolar series-parallel circuits for – 1) charge refreshing, 2) voltage step-up, and 3) inverting. Owing to the cross-switched structure, $C_{(odd)}$ are charged to V_s by conducting the corresponding $T_{(odd)3}$ when forward voltage is applied through T_{03} and T_{06}; on the other hand; similarly, $C_{(even)}$ are charged by conducting the corresponding $T_{(even)3}$ when inverted voltage is applied through T_{04} and T_{05}. Positive voltage is produced across the SC units by conducting T_{x1} and T_{x3}; while negative voltage is produced by conducting T_{x2} and T_{x3}. Besides, the SC units can be by-passed by turning off T_{x3}. The operations of the SC units are illustrated in Fig. 2. By combining the series stacking states, the by-passing states, and also the parallel states, the SCMLI can produce AC output with different voltage levels and balance the capacitor voltages at the same time.

An example of switching states for producing different output voltage levels and the corresponding operations of the capacitors is suggested in table II. The presented topology provides redundant switching states when the output voltage is lower than $\pm(k+1)V_s$. By incorporating different redundant

TABLE II. THE STATES OF THE SWITCHES AND CAPACITORS AT DIFFERENT OUTPUT VOLTAGE LEVELS

Output voltage (V_o)	'ON' switches	Capacitor status
		$C_1, C_2, \cdots, C_{(2n-1)}, C_{(2n)}$
$(2n+1)V_s$	$T_{01}, T_{04}, T_{11}, T_{13}, T_{21}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n-1)3}, T_{(2n)1}, T_{(2n)3}, T_{(2n+1)2}$	D, D, ⋯, D, D
$2nV_s$	$T_{01}, T_{03}, T_{06}, T_{11}, T_{12}, T_{13}, T_{21}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n-1)3}, T_{(2n)1}, T_{(2n)3}, T_{(2n+1)2}$	C, D, ⋯, D, D
	$T_{01}, T_{04}, T_{11}, T_{13}, T_{21}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n-1)3}, T_{(2n)1}, T_{(2n)3}, T_{(2n+1)1}$	D, D, ⋯, D, B
$(2n-1)V_s$	$T_{01}, T_{04}, T_{05}, T_{11}, T_{12}, T_{21}, T_{22}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n-1)3}, T_{(2n)1}, T_{(2n)3}, T_{(2n+1)2}$	B, C, ⋯, D, D
	$T_{01}, T_{04}, T_{11}, T_{13}, T_{21}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n)2}, T_{(2n+1)2}$	D, D, ⋯, B, B
⋮	⋮	⋮
$2V_s$	$T_{01}, T_{03}, T_{06}, T_{11}, T_{12}, T_{13}, T_{21}, T_{22}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)1}, T_{(2n)3}, T_{(2n+1)2}$	C, B, ⋯, C, D
	$T_{01}, T_{04}, T_{11}, T_{13}, T_{21}, \cdots, T_{(2n-1)2}, T_{(2n)1}, T_{(2n+1)1}$	D, B, ⋯, B, B
V_s	$T_{01}, T_{04}, T_{05}, T_{11}, T_{12}, T_{21}, T_{22}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n)1}, T_{(2n)2}, T_{(2n)3}, T_{(2n+1)2}$	B, C, ⋯, B, C
	$T_{01}, T_{03}, T_{06}, T_{11}, T_{12}, T_{13}, T_{21}, T_{22}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)1}, T_{(2n+1)1}$	C, B, ⋯, C, B
0	$T_{01}, T_{04}, T_{05}, T_{11}, T_{12}, T_{21}, T_{22}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n)1}, T_{(2n)2}, T_{(2n)3}, T_{(2n+1)1}$	B, C, ⋯, B, C
	$T_{01}, T_{03}, T_{06}, T_{11}, T_{12}, T_{13}, T_{21}, T_{22}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)2}, T_{(2n+1)2}$	C, B, ⋯, C, B
$-V_s$	$T_{02}, T_{04}, T_{05}, T_{11}, T_{12}, T_{21}, T_{22}, T_{23}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n)1}, T_{(2n)2}, T_{(2n)3}, T_{(2n+1)2}$	B, C, ⋯, B, C
	$T_{02}, T_{03}, T_{06}, T_{11}, T_{12}, T_{13}, T_{21}, T_{22}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)2}, T_{(2n+1)2}$	C, B, ⋯, C, B
$-2V_s$	$T_{02}, T_{03}, T_{06}, T_{11}, T_{12}, T_{13}, T_{21}, T_{22}, \cdots, T_{(2n-1)1}, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)2}, T_{(2n)3}, T_{(2n+1)1}$	C, B, ⋯, C, D
	$T_{02}, T_{05}, T_{12}, T_{13}, T_{22}, \cdots, T_{(2n-1)1}, T_{(2n)2}, T_{(2n+1)2}$	D, B, ⋯, B, B
⋮	⋮	⋮
$-(2n-1)V_s$	$T_{02}, T_{04}, T_{05}, T_{11}, T_{12}, T_{21}, T_{22}, T_{23}, \cdots, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)2}, T_{(2n)3}, T_{(2n+1)1}$	B, C, ⋯, D, D
	$T_{02}, T_{05}, T_{12}, T_{13}, T_{22}, T_{23}, \cdots, T_{(2n-1)2}, T_{(2n)1}, T_{(2n+1)1}$	D, D, ⋯, B, B
$-2nV_s$	$T_{02}, T_{03}, T_{06}, T_{11}, T_{12}, T_{13}, T_{22}, T_{23}, \cdots, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)2}, T_{(2n)3}, T_{(2n+1)1}$	C, D, ⋯, D, D
	$T_{02}, T_{05}, T_{12}, T_{13}, T_{22}, T_{23}, \cdots, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)2}, T_{(2n+1)2}$	D, D, ⋯, D, B
$-(2n+1)V_s$	$T_{02}, T_{05}, T_{12}, T_{13}, T_{22}, T_{23}, \cdots, T_{(2n-1)2}, T_{(2n-1)3}, T_{(2n)2}, T_{(2n)3}, T_{(2n+1)1}$	D, D, ⋯, D, D

*C: Charge; D: Discharge; B: by-passed

switching states, a better load sharing between SC units could be achieved.

III. CAPACITOR VOLTAGE RIPPLES AND LOSS ANALYSIS

The topology employs series-parallel technique to achieve self-balancing of the capacitor voltage. During series operation, the capacitor is discharged at the same magnitude as the output current, i_o. This leads to reduction in the capacitor voltage. When the capacitors are charged during parallel operation, the voltage different between the capacitors and the DC voltage source will cause charge-up power loss [16]. The voltage ripples of the capacitors are determined by the output current, operating frequency, modulation technique, as well as the sizes of the switched-capacitors.

A. Staircase modulation

In this study, a staircase modulation based on the optimal THD technique [17] was adopted to synthesize the AC output with staircase voltage levels. The staircase modulation could be described by (1)

$$\sin\theta_i = \frac{i-0.5}{\rho m(k+1)} \tag{1}$$

where θ_i is the firing angle of the ith voltage level, k is the number of SC units, m is the modulation index, and ρ is the correction factor [17].

B. Voltage ripples of capacitors

The magnitude of the capacitor voltage ripples, ΔV_{ci}, could be estimated with the total amount of discharge during series operation, i.e.

$$\Delta V_{Ci} = \frac{1}{\omega c_i}\int_{\theta_{i(on)}}^{\theta_{i(off)}} i_o d\omega t \tag{2}$$

which can be approximated by the fundamental magnitude of the output current, I_{o1}, and expressed as (3).

$$\Delta V_{Ci} = \frac{I_{o1}}{\omega c_i}\int_{\theta_{i(on)}}^{\theta_{i(off)}} \sin(\omega t-\varphi) d\omega t \tag{3}$$

where c_i is the capacitance of C_i, ω is the fundamental angular frequency of the output voltage, $\theta_{i(on)}$ to $\theta_{i(off)}$ is the conduction angle for series operation of the ith SC unit and φ is the phase angle between the output voltage and current. According (1) and table II, the conduction angles of the ith SC units could be computed with (4).

$$\begin{cases} \theta_{i(on)} = \arcsin\left(\dfrac{i+0.5}{\rho m(k+1)}\right) \\ \theta_{i(off)} = \pi - \arcsin\left(\dfrac{k-i+1.5}{\rho m(k+1)}\right) \end{cases} \tag{4}$$

By substituting (4) into (3), the function of the capacitor voltage ripple would become

$$\Delta V_{Ci} = \frac{I_{o1}}{2\pi f c_i}\left[\cos\varphi\sqrt{1-\alpha_i^2} + \cos\varphi\sqrt{1-\beta_i^2} - \sin\varphi\left(\beta_i - \alpha_i\right)\right] \quad (5)$$

where f is the fundamental frequency of the output voltage, $\alpha_i = \frac{i+0.5}{\rho m(k+1)}$ and $\beta_i = \frac{k-i+1.5}{\rho m(k+1)}$.

Equation (5) indicates that the magnitudes of the capacitor voltage ripples are directly proportional to the output current, i_o, but inversely proportional to the operating frequency and the size of the capacitors. Also, the ripples' magnitudes depends on the power factor of the load and the number of SC units, k.

C. Charge-up power losses of the capacitors

During parallel operation, the capacitors are charged by the DC source through the parasitic resistance of the switches and the ESR of the capacitors. The difference between the DC source voltage and the capacitor voltage would cause energy losses, $E_{loss(Ci)}$ [16]. Assuming that the capacitors are charged to fairly close to V_s, the charge-up losses could be evaluated by comparing the amount of energy removed from the DC source, $E_{in(Ci)}$, and the amount of energy gained in the capacitors, $E_{gain(Ci)}$, throughout the charging process. These could be expressed as following equations.

$$E_{in(Ci)} = c_i V_s \Delta V_{Ci} \quad (6)$$

$$E_{gain(Ci)} = \frac{1}{2} c_i \left[V_s^2 - \left(V_s - \Delta V_{Ci}\right)^2\right] \quad (7)$$

$$E_{loss(Ci)} = E_{in(Ci)} - E_{gain(Ci)} \quad (8)$$

By substituting (6) and (7) into (8), the charge-up energy loss of the i[th] capacitor for a charging cycle is therefore

$$E_{loss(Ci)} = \frac{1}{2} c_i \Delta V_{Ci}^2 \quad (9)$$

In the presented switching scheme, the switched-capacitors are charged at twice of the fundamental output frequency. Hence, the charge-up power losses for a k-unit SCMLI could be calculated by

$$P_{loss(\mathrm{ch})} = \frac{I_{o1}^2}{2\pi f}\sum_{i=1}^{k}\frac{\left[\cos\varphi\sqrt{1-\alpha_i^2} + \cos\varphi\sqrt{1-\beta_i^2} - \sin\varphi\left(\beta_i - \alpha_i\right)\right]^2}{c_i} \quad (10)$$

Referring to (10), the charge-up losses of the SCMLI is directly proportional to the square of the output current magnitude; the efficiency of the SC units could be improved by increasing the operating frequency, f, and the sizes of capacitors, c_i.

TABLE III. COMPARISON OF THE PROPOSED SCMLI WITH EXISTING TOPOLOGIES

Parameter	Topology			
	Fig. 1 in [5]	Fig. 1 in [7]	Fig. 2 in [9]	Proposed
Capacitors	k	k	k	k
Output levels	$2k$+3	$2k$+3	2^{k+1}+1	$2k$+3
$V_{o,max.}$	$(k+1)V_s$	$(k+1)V_s$	2^kV_s	$(k+1)V_s$
Active switches	$3k$+4	k+5	$3k$+3	$3k$+8
Diodes	0	$2k$	k	0
$V_{c,max}$	V_s	V_s	$2^{k-1}V_s$	V_s
$V_{sw,max}$	$(k+1)V_s$	$(k+1)V_s$	2^kV_s	$2V_s$
$V_{D,max}$	N/A	kV_s	$(2^k-1)V_s$	N/A
$V_{sw,tot}$	$(7k+4)V_s$	$(6k+4)V_s$	$(7\cdot2^k-4)V_s$	$(6k+8)V_s$
$V_{D,tot}$	N/A	k^2V_s	$(2^k-k)V_s$	N/A
Inductive load	Yes	Limited ($\varphi < \theta_1$)	Yes	Yes

IV. COMPARISON WITH EXISTING TOPOLOGIES

There are several existing MLI topologies based on the series-parallel conversion technique to achieve self-balancing of the capacitor voltage. In this section, the proposed SCMLI is compared with similar topologies suggested in [5], [7] and [9]. The step-up multilevel inverter suggested in [7] is a variation of [5] and the number of active switches is reduced by rearranging the SC circuits and substituting some of the switches with diodes. A main drawback of that topology is that the ability of driving inductive loads is limited. On the other hand, the switched-capacitor DC/DC converter proposed in [9] allows asymmetric capacitor voltage so that higher number of output levels is available. However, the voltage ratings of the capacitors and the switches would increase dramatically with the growing number of SC units. The topologies suggested in [5] and [7] require an H-bridge at output side to invert the voltage polarity; while [9] proposed a combination of sub-inverters with separated DC sources and half-bridges to produce the bipolar voltage waveform across the output terminals. In order to compare these topologies directly, the SC DC/DC converter presented in [9], cooperating with an H-bridge output stage is employed in this study.

The key parameters, including the number of output levels; maximum output voltage, $V_{o,\ max}$; number of active switches and diodes; maximum voltage ratings of the capacitors, $V_{c,max}$, active switches, $V_{sw,max}$, diodes, $V_{D,max}$; as well as the sum of the voltage ratings of the switches, $V_{sw,tot}$ and $V_{D,tot}$, of the topologies suggested in [5], [7], [9] and the proposed SCMLI, with k SC units and a dc voltage source of V_s, are listed in table III. The proposed topology offers the same number of output levels and maximum output voltage as [5] and [7], which are $2k$+3 and $(k+1)V_s$, respectively; while the topology suggested in [9] offers more number of output levels and higher output voltage, which are 2^{k+1}+1 and 2^kV_s, respectively. However, the voltage ratings of the capacitors, switches and diodes also increase correspondingly. Although all listed topologies are capable of voltage step-up, the active switches in the H-bridge or half-bridge of the existing topologies in

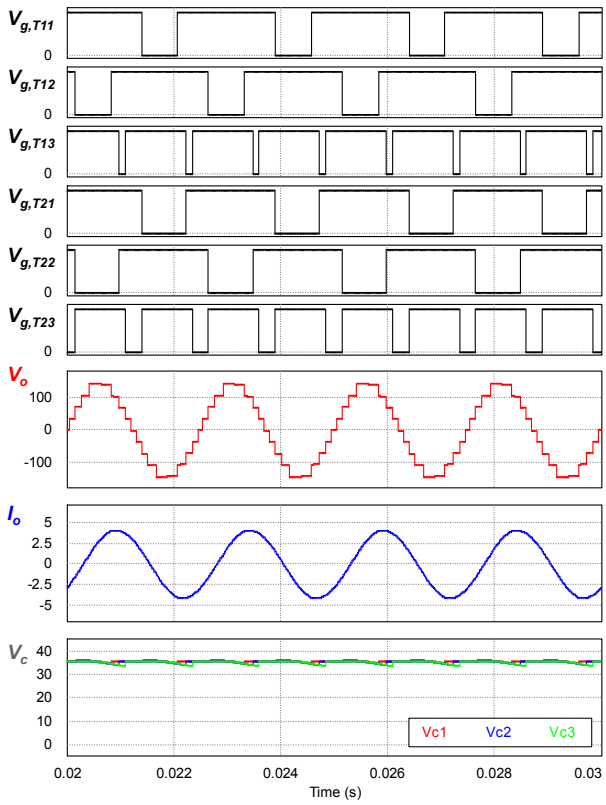

Fig. 3. Simulation result of a 9-level SCMLI; the gate driver signals for the 1st and 2nd SC units; the output voltage, current and the voltages of capacitors

both [5], [7] and [9] require considerable higher voltage ratings of $V_{o,\,max}$, in comparison to the proposed topology.

V. Simulation and Experiment Results

In order to validate the operation of the proposed topology, an ideal 9-level MLI with 36V source voltage and four 1000µF SC units, operating at 400Hz with optimal THD staircase modulation [17], was simulated. The output and capacitor voltage, as well as the voltage stress of the switches under inductive load of 25Ω-10mH were analyzed. The simulated waveforms, including the selected gate driver signals, the output voltage and current, as well as the voltage of the switched-capacitors, are depicted in Fig. 3. The simulated waveforms show peak output voltage and current of approximately 144V and 4A, respectively; while the maximum voltage stress of the switches T_{11} to T_{23} was about 72V. Since the load was inductive ($\varphi \approx 45°$) in the simulation model, the voltage ripples increased with SC number i. The simulated voltage ripples of the capacitors were varied from around 1.06V to 2.2V.

Besides, a 9-level MLI prototype, employing the proposed topology with three 1000µF SC units, was built. The capacitor voltage and output waveforms (Fig. 4) under different operating frequencies and loading conditions were measured. The results suggested that the inverter has greater power output capability and lower capacitor voltage ripples at higher operating frequency, similar to other SCMLIs as expected.

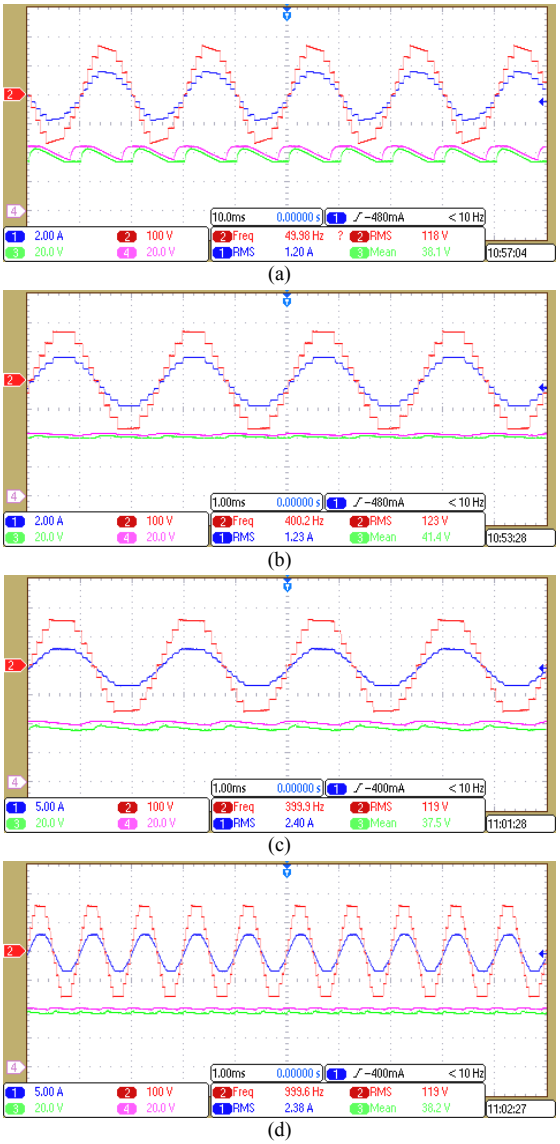

Fig. 4. Measurements of the 9-level SCMLI prototype (CH1: V_o; CH2: i_o; CH3: V_{c1}; CH4: V_{c2}); (a) driving a 100Ω-1mH load at 50Hz; (b) 100Ω-1mH load at 400Hz; (c) 50Ω-1mH load at 400Hz; (d) 50Ω-1mH load at 1kHz

Compared with the capacitor waveforms in Fig. 3 which were simulated under ideal condition, the charging rate of the capacitors in the experiment was limited by the ESR of the capacitors and the parasitic resistance and inductance of the circuit layout. This would limit the maximum operating frequency of the SCMLI.

VI. Conclusion

A novel SCMLI topology, which strikes the balance between component count and voltage ratings by cooperating the bipolar SC technique with cross-switched structure, has been proposed. By enabling the modular approach, the presented topology offers a potential alternative for scalable and high step-up DC/AC applications. Moreover, identical SC modules are more preferable for mass production and

maintenance, which substantially reduces the system and operation cost. This paper suggests the selection of the redundant switching states, as well as provides the analyses in SC voltage ripples and the associated energy losses, considering different operating frequencies, loading conditions and component sizes. Operation of the SCMLI with staircase modulation was verified by the simulation and experiment results. The analyses and results suggest that the presented SCMLI is more favorable for high frequency applications such as the 400-Hz systems or other power systems operating at a few kilohertz.

ACKNOWLEDGMENT

The authors wish to acknowledge the support provided by the members of the Power Electronics Research Centre (PERC) and Research Committee at The Hong Kong Polytechnic University.

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