This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2457454, IEEE Transactions on Power Electronics

High-Gain Single-Stage Boosting Inverter for Photovoltaic Applications

Alexander Abramovitz, *Member IEEE*, Ben Zhao, *Student Member*, and Keyue Smedley, *Fellow IEEE*

***Abstract*— This paper introduces a high gain Single-Stage Boosting Inverter (SSBI) for alternative energy generation. As compared to the traditional two stage approach, the SSBI has a simpler topology and a lower component count. One Cycle Control was employed to generate AC voltage output. The paper presents theoretical analysis, simulation and experimental results obtained from a 200W prototype. The experimental results reveal that the proposed SSBI can achieve high DC input voltage boosting, good DC-AC power decoupling, good quality of AC output waveform, and good conversion efficiency.**

***Index Terms*—micro-inverter, tapped-inductor, OCC.**

I. Introduction

Micro inverter topologies for PV power generation are classified into three major groups [1]: the single-stage, the two-stage and the multi-stage types. The multi-stage micro-inverters are usually comprised of a step-up DC-DC converter front stage, under Maximum Power Point Tracking (MPPT) control, an intermediate high frequency DC-DC converter stage, used to attain a rectified-sine waveform, and a low frequency unfolding stage to interconnect to the grid [2], [3]. However, the multi-stage power train and the associated high component count results in a costly product [4]. The two-stage micro-inverter can be designed cascading a MPPT controlled step-up DC-DC converter and a grid tied high frequency inverter. Whereas the single-stage topology has to perform the voltage step-up, the MPP tracking, and the DC-AC inversion functions all in one stage.

In order to convert and connect the solar energy to the grid the low voltage of the PV panel first has to be stepped-up significantly to match the utility level. This poses a challenge to the designer of photovoltaic inverters as the traditional boost converter cannot provide the required gain at high efficiency. Therefore, an extensive research effort is dedicated to developing various topologies of high step up DC-DC converters [5]-[7] that can be used in tandem with a half or full bridge inverter [8] to implement a solar power generation system.

Another concern, typical to single phase DC-AC power systems, is AC-DC power decoupling problem. A traditional solution is application of a decoupling capacitor on the DC link between the input and output stages. The value of the decoupling capacitor depends on the rated power, P_{dc}, the line frequency, f, the average voltage across the capacitor, V_{dc}, and the allowed peak-to-peak ripple, $\triangle v$, [9]:

$$C_{dc} = \frac{P_{dc}}{2\pi f V_{dc} \Delta v} \quad (1)$$

The two-stage or the multi-stage micro-inverters can have their decoupling capacitor on the high voltage DC link, and, according to (1), attain lower value of the decoupling capacitor [9]. However, some single stage micro-inverters may require placing the decoupling capacitor at the PV module terminals. The low panel voltage, V_{dc}, and the desired low ripple, $\triangle v$, see (1), result in a substantial decoupling capacitor value and size (e.g. 2.4mF for V_{dc}=35V, $\triangle v$=6V, and P_{dc}=160W [1]). In field conditions large electrolytic capacitors have short life and impair system's reliability. Therefore, the power decoupling problem becomes one of major concerns in micro-inverter design. Application of small non electrolytic capacitors is strongly desired. To minimize the decoupling capacitor, an additional power decoupling circuits were suggested in literature. A flyback-type single stage topology with an additional power decoupling circuit proposed in [10] reported a decoupling capacitor of only 40uF. However, the efficiency was only 70%. An improved topology employing leakage energy recycling [11] demonstrated 86% peak efficiency. Some other flyback based topologies [12]-[14] also make use of an additional power decoupling circuit.

Single stage topologies that can realize voltage step-up and inversion in a single stage were proposed in the past. In [15], a dual boost inverter was suggested. Here the load is connected differentially between the outputs of two bi-directional boost converters, see Fig. 1. As a result the topology resembles a common H-bridge with the boosting inductors connected to the legs' midpoints. The demerits of this approach are the limited DC step-up gain; circulating currents, which impair the efficiency; and somewhat complicated control. Since the function of C_1 and C_2 is merely output filtering the decoupling capacitor should be placed at the low voltage input, which is an additional disadvantage. Another single stage solution [16], [17] is shown in Fig. 2. Compared to [15] the topologies in [16], [17] use a single boost inductor; have no circulating currents; have a high voltage DC link and, accordingly, a smaller decoupling capacitor. Also, traditional control methods can be applied.

Moreover, the topologies proposed in [18], [19] may provide other choices for single stage solutions. However, the limited DC step-up of [15]-[19] necessitates using a more expensive high voltage PV panels with 70-100VDC output in order to get the desired dc bus voltage compatible to grid connected inverters. Alternatively, using the popular crystalline silicon

This paragraph of the first footnote will contain the date on which you submitted your paper for review. It will also contain support information, including sponsor and financial support acknowledgment. For example, "This work was supported in part by the U.S. Department of Commerce under Grant BS123456".

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2457454, IEEE Transactions on Power Electronics

modules with the 25-50VDC MPP range, these topologies can implement a two-three panel string inverter, which, as any string architecture, is prone to the mismatch problem.

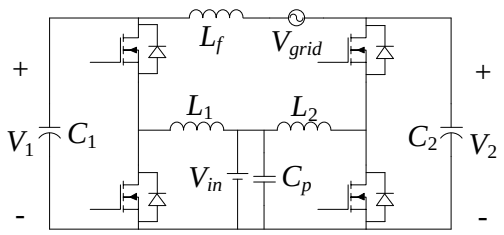


Fig. 1. Topology presented in [15].

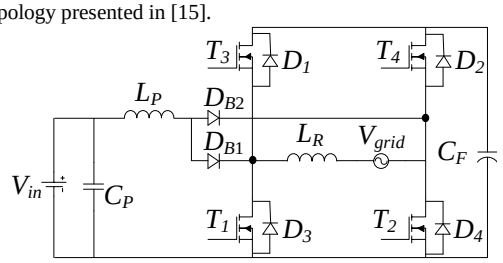


Fig. 2. Topology presented in [17].

In this paper a Single-Stage Boosting Inverter (SSBI) is proposed for alternative energy/solar power generation. SSBI can be regarded as further improvement of [16] and [17]. SSBI can attain higher DC gain and, thus, operate off low DC input voltage of a single PV panel. By its concept of operation SSBI shares the switches of the power train in a manner that allows merging the DC-DC step up converter stage and the grid tied DC-AC inverter stage. Hence, SSBI is realized in a single stage. The power decoupling is performed at high voltage, thus, low value of DC link decoupling capacitor is required. The SSBI easily lends itself to application of One Cycle Control (OCC), which helps attaining high quality AC output regardless of low frequency ripple across the DC link. However, any other control method can be applied. The paper presents theoretical analysis, simulation and experimental results obtained from a stand-alone 200W prototype.

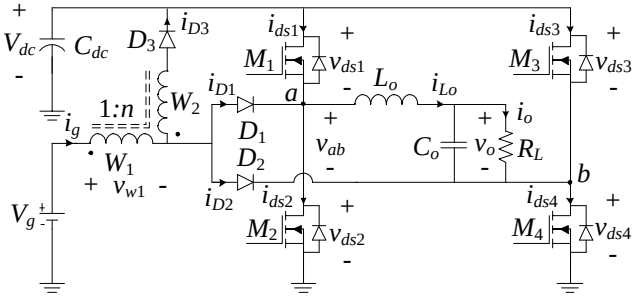


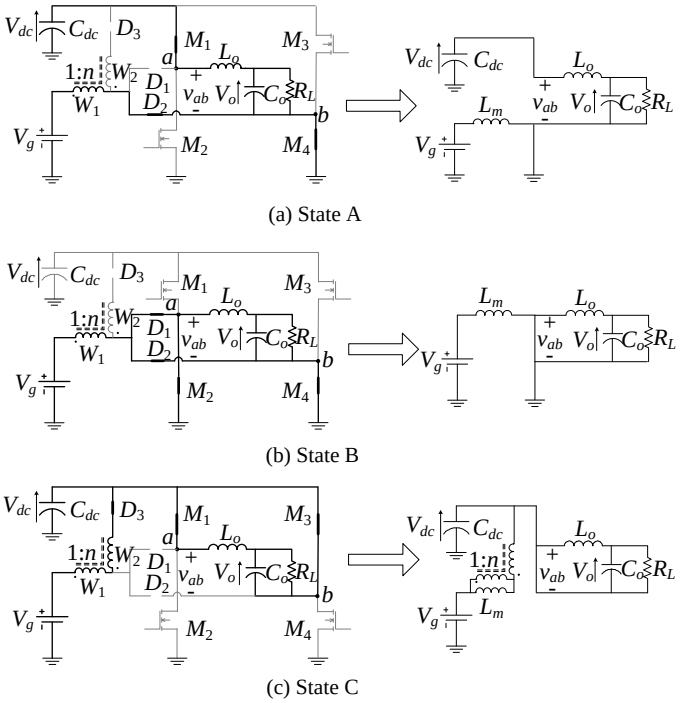
Fig. 3. Topology of the proposed Single Stage Boosting Inverter.

II. Description of The Proposed Topology

The proposed schematic diagram of the proposed SSBI is given in Fig. 3, which is an improvement of the scheme given in [16, 17]. SSBI is comprised of semiconductor switches $M_{1\ldots4}$, arranged in a full bridge configuration; steering diodes $D_{1,2}$; DC link diode D_3, the tapped inductor W_1:W_2; the decoupling capacitor C_{dc}; and the output filter L_o-C_o. The load is represented by the resistor R_L. The proposed SSBI is fed by a DC voltage source, V_g, considered to be derived of a single PV panel, and generates utility level AC output voltage V_o. Here, the input current is designated as i_g, the output current is i_o and its average component is I_o.

Compared to [16], [17] the proposed SSBI topology has the advantages of a larger voltage step-up which can be achieved adjusting the tapped inductor turns ratio, and smaller decoupling capacitor, which is placed on high voltage dc bus.

Principle of operation of the proposed SSBI is hinged on implementation of a specialized switching pattern of the H-bridge. In order to generate output voltage of positive polarity, three topological states are created during the switching cycle as shown in Fig. 4. Here, buck and boost sub-topologies can be identified.



(a) State A

(b) State B

(c) State C

Fig. 4. Topological states of the proposed SSBI and their equivalent circuits.

The switching cycle starts with *State A*, shown in Fig. 4 (a), which lasts for a duration of t_a. Here, the switches M_1 and M_4 are on, whereas switches M_2 and M_3 are off, D_2 conducts and D_1, D_3 are cut-off. During this state the tapped inductor primary magnetizing inductance, L_m, is charged from the input voltage source, V_g, while the DC voltage, V_{dc}, is applied to the input terminals of the output filter so the filter inductance, L_o, is charged feeding also the filter capacitor, C_o, and the load R_L.

State B, see Fig. 4 (b), commences, as the switch M_1 is turned off and M_2 is turned on, whereas M_4 keeps conducting. State B lasts for a duration of t_b. Here, both D_1 and D_2 conduct while D_3 is cut-off. As a result, the tapped inductor magnetizing inductance, L_m, continues charging from the input voltage source, V_g, whereas the input terminals of the output filter are shorted so the filter inductance, L_o, is discharged to the output capacitor C_o and the load R_L.

State C, see Fig. 4 (c), begins as the switches M_1, M_3 are turned on and M_2, M_4 are turned off. State C lasts for duration of

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2457454, IEEE Transactions on Power Electronics

t_c, and completes the switching cycle. Here, both D_1, D_2 are cut-off and D_3 conducts; the tapped inductor magnetizing inductance, L_m, is discharged via both windings and D_3 into the DC link capacitor, C_{dc}, while the input terminals of the output filter are shorted and the filter inductance, L_o, feeds the output capacitor, C_o, and the load R_L.

In order to generate output voltage of negative polarity, complementary switching states A', B', C' are created by the controller. Switching states of semiconductor devices throughout the switching cycle are summarized in Table I.

TABLE I
SWITCHING STATES OF SEMICONDUCTOR DEVICES

	Positive Output Voltage			Negative Output Voltage		
	State A	State B	State C	State A'	State B'	State C'
M_1	ON	OFF	ON	OFF	OFF	ON
M_2	OFF	ON	OFF	ON	ON	OFF
M_3	OFF	OFF	ON	ON	OFF	ON
M_4	ON	ON	OFF	OFF	ON	OFF
D_1	OFF	ON	OFF	ON	ON	OFF
D_2	ON	ON	OFF	OFF	ON	OFF
D_3	OFF	OFF	ON	OFF	OFF	ON

To create the desired switching states, proper switching signals for the H-bridge switches should be generated of the given buck and boost switching functions and the output polarity signal $S_{bk}(D_{bk})$, $S_{bst}(D_{bst})$, P, respectively. Here, the driving signals of the switches $M_1 \ldots M_4$ are designated as $S_1 \ldots S_4$ respectively. The required Boolean functions can be derived from Table I

$$\begin{aligned} S_1 &= \overline{\overline{P \cdot S_{bk}} \cdot S_{bst}} \\ S_2 &= \overline{P \cdot S_{bk}} \cdot S_{bst} \\ S_3 &= \overline{\overline{P} \cdot S_{bk}} \cdot S_{bst} \\ S_4 &= \overline{\overline{P} \cdot S_{bk}} \cdot S_{bst} \end{aligned} \tag{2}$$

Key waveforms of the proposed SSBI throughout a line frequency cycle are illustrated in Fig. 5.

Note that since the switching cycle of SSBI is comprised of three states, there are 3! possible permutations or state sequences. In other words, the order of appearance of the states is not unique and other possibilities exist, i. e. A-C-B, C-B-A etc. An ideal SSBI can generate same DC-DC conversion ratio under any of these switching regimes. However, some state sequences may require switches to be activated twice per switching cycle, which is undesirable in practice due to increased switching loss and/or extremely narrow on time. Proper synchronization of the gating signals also requires attention. The advantage of the implemented A-B-C state sequence is that each switch is turned on and off only once in a switching cycle, which helps reducing the switching losses.

As a result of the proposed switching strategy the voltage, v_{ab}, at the input terminals of the output filter is a three level pulse train, which can be properly modulated to generate the desired output waveform of either polarity as shown in Fig. 5.

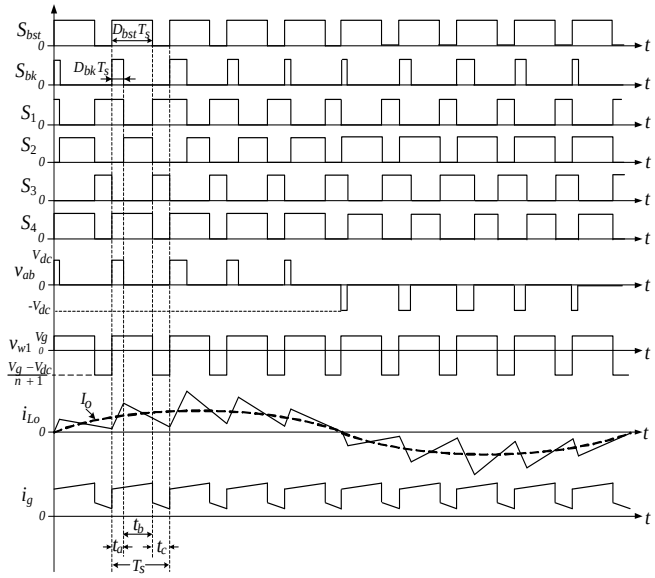


Fig. 5. Key waveforms of the proposed SSBI.

III. SSBI ANALYSIS AND SIMULATION

To facilitate the analysis approach the following assumptions are adopted: (a) all semiconductors are ideal with zero on resistance and voltage drop; (b) the decoupling capacitor and the output filter capacitor are sufficiently large and their voltage ripple is negligible; (c) continuous current operation of both the tapped inductor and the output filter inductor is assumed.

A. Derivation of Voltage Conversion Ratio

Inspection of the converter's equivalent circuits in Fig. 4 reveals that the power stage operates as a boost-derived tapped inductor DC-DC converter merged with a buck-derived full-bridge DC-AC inverter.

Define t_a, t_b, and t_c the duration of states A, B and C respectively and $T_s=t_a+t_b+t_c$ the switching period. Boost charging state, that is the time interval dedicated to charging the primary winding of the tapped inductor, takes place during the states A and B, see Fig. 4 (a) and Fig. 4 (b), whereas, boost discharge takes place in state C. The total duration of the boost charging is, therefore:

$$t_{bst} = t_a + t_b \tag{3}$$

Accordingly, the resulting boost duty cycle, D_{bst}, is

$$D_{bst} = \frac{t_a + t_b}{T_s} \tag{4}$$

Hence, SSBI performs the DC-DC step-up conversion function identically to the tapped inductor boost converter. Adopting the approach of [20] and [21], the DC-DC voltage conversion ratio of SSBI is

$$M_{bst} = \frac{V_{dc}}{V_g} = \frac{1 + nD_{bst}}{1 - D_{bst}} \tag{5}$$

The voltage conversion ratio (5) is plotted in Fig. 6. Clearly, by adjusting the turn ratio, n, the proposed SSBI can achieve higher conversion ratio than a traditional boost converter.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2457454, IEEE Transactions on Power Electronics

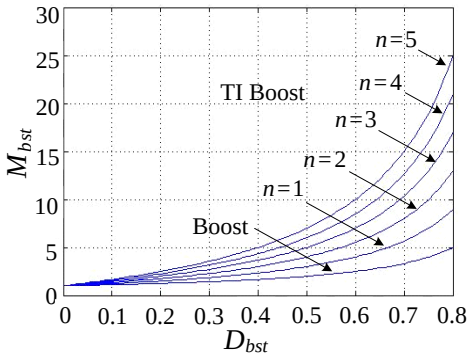


Fig. 6. Comparison of conversion ratio, M_{bst}, of the traditional boost and the tapped inductor (TI) boost converters.

According to the state description above, the buck charging state, that is, the time interval dedicated to charging the output inductor, L_o, occurs in state A, whereas buck discharge takes place in states B and C while the terminals of the output filter are shorted. Thus, the duration of the buck charging is:

$$t_{bk} = t_a \tag{6}$$

Accordingly, the resulting buck duty cycle, D_{bk}, is

$$D_{bk} = \frac{t_a}{T_s} \tag{7}$$

Clearly, under CCM condition of the output filter inductor, the voltage gain of the output section is identical to that of a buck converter and is given by:

$$M_{bk} = \frac{V_o}{V_{dc}} = D_{bk} \tag{8}$$

Hence, the overall DC-AC voltage conversion ratio, M, of the proposed SSBI under CCM conditions can be derived combining (5) and (8):

$$M = \frac{V_o}{V_g} = M_{bk} M_{bst} = \frac{(1+nD_{bst})D_{bk}}{1-D_{bst}} \tag{9}$$

In stand-alone application the buck duty ratio, D_{bk}, is modulated to attain a sinusoidal output voltage, V_o, of required amplitude and frequency, whereas the boost duty ratio, D_{bst}, is adjusted to satisfy load power demand and so stabilize the DC link voltage, V_{dc}. However, an important constrain arising from SSBI principle of operation is that the buck duty ratio, D_{bk}, should be smaller than the boost duty ratio, D_{bst}, at all times: $D_{bk} < D_{bst}$.

B. *Voltage and current Stress of semiconductor devices*

Peak voltage and peak current of the semiconductor devices during a switching cycle are summarized in Table II. The values of the RMS currents of the semiconductor devices throughout the line cycle are given in Table III. Here, the RMS value of buck duty cycle is defined as $D_{bkrms} = D_{bkm}/\sqrt{2}$.

TABLE II.
PEAK VOLTAGE AND CURRENT STRESSES PER SWITCHING CYCLE

	Peak Voltage	Peak Current
M_1	V_{dc}	I_{omax}
M_2	V_{dc}	$I_{g1max}+I_{omax}$
M_3	V_{dc}	I_{omax}
M_4	V_{dc}	$I_{g1max}+I_{omax}$
D_1	V_{dc}	I_{g1max}
D_2	V_{dc}	I_{g1max}
D_3	$V_{dc}+nV_g$	I_{g2max}

TABLE III.
RMS CURRENT STRESSES PER LINE CYCLE

$\frac{I_{ds1RMS}}{I_{orms}}, \frac{I_{ds3RMS}}{I_{orms}}$	$\sqrt{\frac{4\sqrt{2}D_{bkrms}}{3\pi} - D_{bst} + 1}$
$\frac{I_{ds2RMS}}{I_{orms}}, \frac{I_{ds4RMS}}{I_{orms}}$	$\sqrt{\frac{(n+1)^2 D_{bkrms}^2 \left(\pi D_{bst} + 2\sqrt{2}D_{bkrms}\right)}{4\pi(1-D_{bst})^2} + \frac{(n+1)D_{bkrms}^2}{1-D_{bst}} + \frac{4\sqrt{2}D_{bkrms}}{3\pi}}$
$\frac{I_{D1RMS}}{I_{orms}}, \frac{I_{D2RMS}}{I_{orms}}$	$\sqrt{\frac{(n+1)^2 D_{bkrms}^2 \left(\pi D_{bst} + 2\sqrt{2}D_{bkrms}\right)}{4\pi(1-D_{bst})^2} - \frac{8\sqrt{2}D_{bkrms}}{3\pi} + D_{bst}}$
$\frac{I_{D3RMS}}{I_{orms}}$	$\frac{D_{bkrms}}{\sqrt{1-D_{bst}}}$

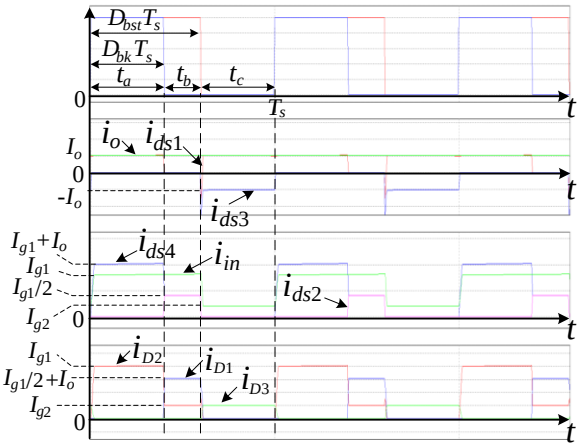


Fig. 7. Simulated waveforms of the proposed SSBI on the switching frequency scale during positive half cycle.

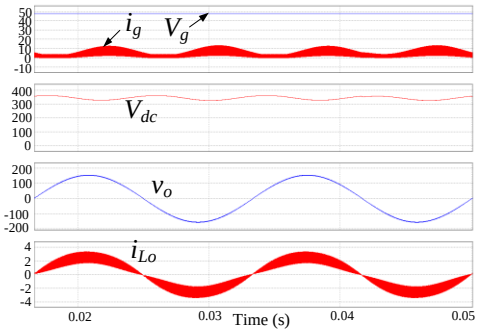


Fig. 8. Simulated waveforms of the proposed SSBI on the line frequency scale.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2457454, IEEE Transactions on Power Electronics

C. Simulation Results

A stand-alone variant of the proposed SSBI and its OCC control circuits were implemented for preliminary study using PSIM Version 9.1 software. Simulation waveforms in Fig. 7 reveal the details of SSBI operation on the switching frequency scale, which support the theoretical predictions. Fig. 8 illustrates the principal SSBI waveforms on line frequency scale and confirms that under the OCC control the proposed SSBI can provide high DC input voltage step-up as well as high quality AC output. The advantage of the OCC control can be now clearly observed: due to the superior transient response of the OCC controller, the substantial ripple component of the DC link voltage has no detrimental effect on the quality of the AC output. Hence, lower decoupling capacitor can be employed without compromising DC-AC decoupling. Another advantage of the proposed approach is that the OCC controller required no sensing of the AC output voltage. Hence, there is no need for isolated floating sensors, which further simplifies the circuitry. Detailed description of OCC controller can be found in [22], [23].

IV. DCM Analysis

A. Derivation of the DCM Boost Conversion Ratio

Due to changing environmental conditions the average PV output power can drop significantly. As a result SSBI can enter discontinuous conduction mode (DCM) of the tapped inductor. This operation regime is investigated further.

In the following analysis it is assumed that SSBI is ideal (lossless components) and that the DC link voltage, V_{dc}, is regulated in closed loop to a constant value. The AC-DC power balance suggests that the ac load is reflected to the DC link and can be modeled by an equivalent DC link resistance R_{eq}:

$$R_{eq} = \frac{V_{dc}^2}{P_o} \tag{10}$$

where, P_o is the average power level of the SSBI.

Since the principle of the DC-DC voltage step-up of the proposed SSBI is similar to that of the tapped inductor boost converter, the model in Fig. 9 is appropriate for investigation of the DCM mode in SSBI. Here, the tapped inductor is modeled as an auto-transformer with a moderately low magnetizing inductance L_m. Typical waveforms of the input current i_g(t) and diode current i_D(t) in the discontinuous conduction mode are illustrated in Fig. 10, where V_{gs} is the driving signal of the switch M, i_{pk} is the peak current of the input current i_g(t) and, I_D is the average diode current.

The volt-second balance of the magnetizing inductance, L_m, suggests

$$\frac{V_{dc}}{V_g} = \frac{(n+1)D_{bst} + D_d}{D_d} \tag{11}$$

where D_{bst} is the switch duty cycle, D_d is the diode duty cycle and D_i is the idle duty cycle as illustrated in Fig. 10.

Charge balance of the output capacitor, C_{dc}, requires the average current of i_D(t) equals the average load current, V_{dc}/R_{eq}, hence,

$$\frac{1}{T_s}\int_0^{T_s} i_D(t)dt = \frac{1}{T_s}\cdot\frac{1}{2}\frac{I_{pk}}{n+1}\cdot D_d T_s = \frac{V_{dc}}{R_{eq}} \tag{12}$$

where, the peak inductor current, I_{pk} is:

$$I_{pk} = \frac{V_g}{L_m} D_{bst} T_s \tag{13}$$

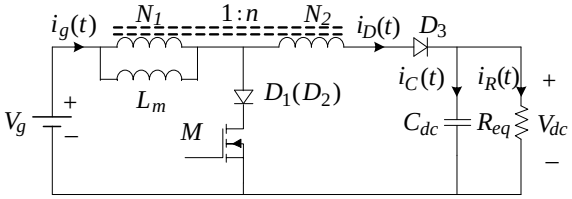


Fig. 9. Input voltage step–up scheme of the proposed SSBI (is identical to the tapped inductor boost converter).

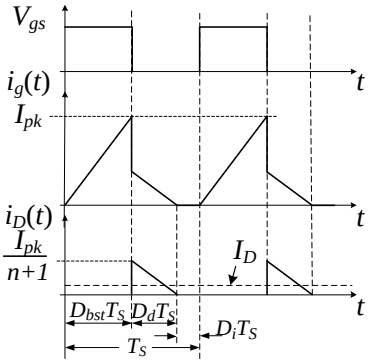


Fig.10. Typical waveforms of the input current i_g(t) and the diode current i_D(t) in DCM.

Substituting (13) to (12), yields:

$$\frac{D_{bst}D_d V_g T_s}{2(n+1)L_m} = \frac{V_{dc}}{R_{eq}} \tag{14}$$

Using (11) and (14), eliminating D_d and solving for V_{dc}, results in:

$$M = \frac{V_{dc}}{V_g} = \frac{1+\sqrt{1+4D_{bst}^2/K}}{2} \tag{15}$$

Where, $K=2L_m/R_{eq}T_s$.

This result is identical to the case of a traditional boost converter [24].

B. CCM-DCM Boundary

The output power level, P_{ob}, which brings the tapped inductor to the CCM-DCM boundary, can be obtained by substituting D_2=1-D_{bst} and (10) into (11) and (14):

$$P_{ob} = \frac{D_{bst}T_s(1+nD_{bst})V_g^2}{2(n+1)L_m} = \frac{D_{bst}(1-D_{bst})^2 T_s V_{dc}^2}{2(n+1)(1+nD_{bst})L_m} \tag{16}$$

C. Minimum Output Power

The boost duty cycle, D_{bst}, can be expressed as function of output power, P_o, using (10) and (15)

$$D_{bst} = \sqrt{\frac{2L_m P_o (V_{dc} - V_g)}{V_{dc} V_g^2 T_s}} \tag{17}$$

Therefore, in DCM and under decreasing load power, in order to keep the DC link voltage, V_{dc}, at constant level the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2457454, IEEE Transactions on Power Electronics

controller has to decrease D_{bst} duty cycle, which may restrict the maximum available buck duty cycle, D_{bkm}, and violate the SSBI requirement $D_{bst}>D_{bkm}=V_{acmax}/V_{dc}$ needed to generate the full output voltage swing. This limitation results in distorted output voltage V_{ac}, which appears flat as if "shaved" at its peak. At the limit of distortion $D_{bst}=D_{bkm}=V_{acmax}/V_{dc}$. Therefore, to avoid distortion SSBI should be presented with the minimum output power, P_{omin},

$$P_{o\min}=\frac{V_{ac\max}^2 V_g^2 T_s}{2L_m V_{dc}\left(V_{dc}-V_g\right)} \tag{18}$$

The boost duty cycle, D_{bst}, is plotted as function of the output power P_o in Fig. 11 for the following set of parameters V_g=48V, V_{dc}=380V, n=3, L_m=150μH, T_s=20μs. Evidently, D_{bst} is constant in CCM and, according to (5) equals D_{bst}(CCM)=0.64. The DCM duty cycle, can be calculated from (17) as $D_{bst}=\sqrt{0.0057P_o}$. The DCM-CCM boundary power P_{ob} =68.36W was calculated from (16). Fig. 11 also illustrates that the $D_{bst}=D_{bkm}$ condition occurs at the minimum output power, P_{omin}. Under lighter loading, $P_o<P_{omin}$, the restricted D_{bkm} causes peak-shaving distortion of the output voltage waveform.

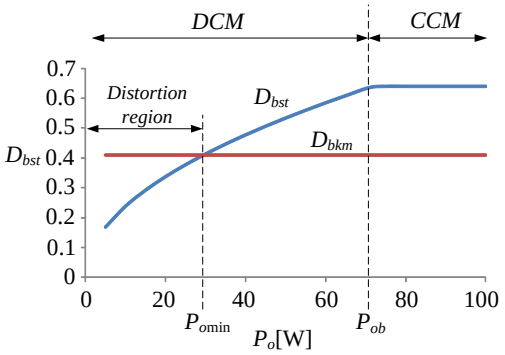


Fig. 11. Variation of the boost duty cycle, D_{bst}, as function of power level, P_o.

D. Verification of DCM Analysis

PSIM simulation was used to verify the DCM voltage conversion ratio (15). The simulation parameters were: V_g=48V, L_m=150μH, T_s=20μs, D_{bst}=0.64, n=3, R_{eq}=4000Ω. Plugging these parameters into (15), yields M_{cal}=10.96, whereas the simulated result is M_{sim}=10.58 strongly supporting the theoretical expectation.

The CCM-DCM boundary condition (16) was verified by simulation using the following parameters: V_g=48V, L_m=150μH, T_s=20μs, D_{bst}=0.64, n=3. The exploded view of the input current, I_g, shown in Fig. 12, clearly indicates that SSBI is indeed at the CCM-DCM boundary. The simulated output power was found as P_{ob}=67W and matched the theoretically expected value of P_{ob}=68.36W calculated from (16).

The simulated waveforms in Fig. 13 illustrate the quality of the output voltage above and below P_{omin}. In Fig. 13 (a) P_o is just above P_{omin} and causes no distortion. In Fig. 13 (b) P_o is just below P_{omin}, and the onset of the peak-shaving distortion can be observed in the output voltage waveform. The parameters used in simulation were: V_g=48V, V_{dc}=380V, V_{acmax}=155.5V, L_m=150μH, T_s=20μs, n=3. Here, the simulated minimum output power, P_{omin}, is 31W as compared to 29.4W predicted by (18).

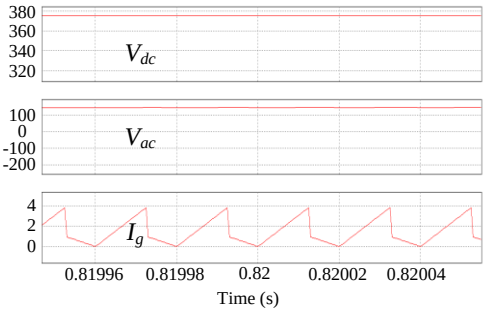


Fig. 12. Simulated waveforms of the SSBI's output voltage, V_{ac}, DC link voltage, V_{dc}, and DC input source current, I_g, with the tapped inductor operating at the CCM-DCM boundary ($P_o=P_{ob}$).

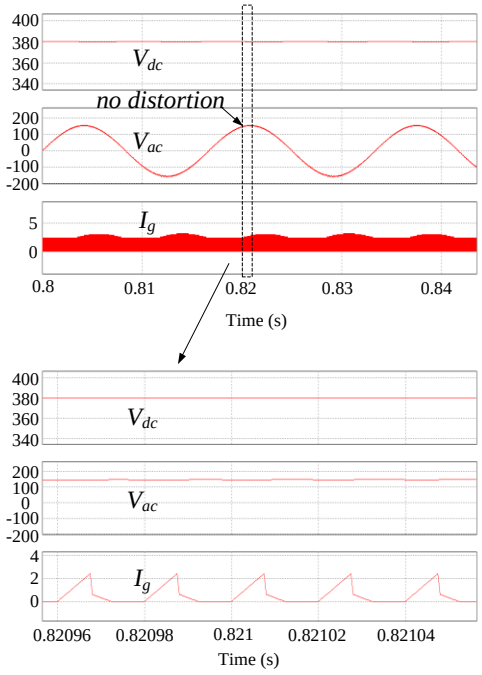


Fig. 13. Simulated waveforms of the SSBI's output voltage, V_{ac}, DC link voltage, V_{dc}, and DC input source current, I_g: (a) illustrating the undistorted output voltage, V_{ac}, when SSBI is operated in deep DCM just above the minimum power level $P_o>P_{omin}$; (b) illustrating the peak-shaving distortion of the output voltage, V_{ac}, for $P_o<P_{omin}$.

V. EXPERIMENTAL RESULTS

Experimental stand-alone prototype SSBI was built and tested. The prototype was designed for a 200W power output; 35-48V DC input; 110V AC output voltage. The switching frequency was set to 50kHz. The OCC controller and timing

circuits were implemented using standard analog and logic chips. The key components of the SSBI prototype were M_1-M_4: SCT2080KE; D_1-D_2: STTH30L06; D_3: C3D04065A; decoupling capacitor C_{dc}: 47μF//450V; tapped inductor turns ratio were: 1:3 for the 48V input unit and 1:4 for the 35V input unit, magnetizing inductance 150μH; output filter inductance L_o: 1mH; output filter capacitance C_o: 1.5μF; Magnetics' cores: C058439A2 and C058254A2 were used. Boost signals were generated with a simple PWM controller UC3824. Fast comparator AD8561 was used to implement the OCC. The experimental work was aimed to verify the principles of the proposed approach. No optimization was attempted.

The experimental waveforms are presented in Figs. 14 - Fig. 17. Fig. 14 shows the waveforms of input and output voltage, along with the output inductor current. The measurements were taken at three different power levels at constant input voltage. SSBI generated high quality AC output voltage in a wide range of output power. Several different load types were presented to SSBI. Fig. 15 shows the waveforms of the output voltage and output current under three different load conditions: (a) linear RL load; (b) non-linear load case I: diode bridge with RC load; (c) non-linear load case II: resistor and a saturable reactor load. The measured THD of the output voltage was 4.98%, 8.5%, and 4% respectively. Fig. 16 shows the input current and the voltage across the switches M_1 and M_2 at negative and positive output cycle. Notice that, in the negative output cycle, the switch M_2 is turned on during the entire boost duty cycle, which represents the input current changing with the switching of the M_2, as shown in Fig. 16 (a). Whereas, in the positive output cycle, the switch M_2 is turned on only part of the boost duty cycle, which represents that the input current begins increasing before the M_2 turned on, as shown in Fig. 16 (b). Fig. 17 (a) shows the key waveforms of the duty cycle generator: the OCC ramp, the AC reference, buck and boost switching signals, S_{bk} and S_{bst}, along with the input current, I_g, and the output inductor current, I_{Lo}. Whereas Fig. 17(b) illustrates the relationship of the buck and boost switching functions S_{bk} and S_{bst} and the derived MOSFET driving signals $S_1 \ldots S_4$ which are consistent with Fig. 5 above.

Two sets of efficiency measurements were taken for two different input voltages: 35VDC and 48VDC. The resultant efficiency plots are illustrated in Fig. 18, as function of the output power. Peak efficiency of 89.3% was achieved. At relatively low input voltage level, the conduction losses of the steering diodes, D_1 and D_2 were identified as the major cause of efficiency drop. However, since it is a rather common practice to install a blocking diode in series with a PV panel to prevent back flow, such configuration and the associated losses are comparable to some other approaches.

Comparison of the proposed SSBI with a number of selected single- and two-stage topologies mentioned in [25] is presented in Table IV. Among the single stage topologies SSBI has the best efficiency performance. Another conclusion arises when these two classes are compared. Evidently, it is a choice of performance vs. cost: two-stage inverters attain better efficiency; however, at the expense of using about twice the number of active switches than the single-stage topologies. In particular, [34] compares a single stage flyback based micro-inverter is compared with a full bridge based two-stage topology. The former has a total of 3 switches and 2 diodes, whereas the latter used 8 switches and 4 diodes yet, the reported efficiency was 84.7% and 92.5% respectively.

TABLE IV
BRIEF COMPARISON OF SINGLE- AND TWO- STAGE TOPOLOGIES

Class	Topology	Sw	D	Vin [V]	Pout [W]	max. Eff. [%]
Single-stage	SSBI	4	3	35-48	200	89.3
	[26]	4	2	48	500	80
	[27]	4	2	90	300	87
	[28]	6	0	30	50	87
	[29]	5	3	92	170	87
Two-stage	[30]	7	3	22-40	250	92
	[31]	6	2	31-51	210	98.2
	[32]	8	2	38-50	2000	93.9
	[33]	6	2	20	250	93

VI. CONCLUSION

A high gain single-stage boosting inverter, SSBI, for alternative energy generation applications is presented in this paper. The proposed topology employs a tapped inductor to attain high input voltage step-up and, consequently, allows operation from low DC input voltage.

The paper presented principles of operation, theoretical analysis of continuous and discontinuous modes including gain and voltage and current stresses.

To facilitate this report two stand-alone prototypes one for 48 V input and another for 35 V input were built and experimentally tested. Theoretical findings stand in good agreement with simulation and experimental results. Acceptable efficiency was attained with low voltage input source.

The proposed SSBI topology has the advantage of high voltage step-up which can be further increased adjusting the tapped inductor turns ratio. The SSBI allows decoupled control functions. By adjusting the boost duty cycle D_{bst} the SSBI can control the dc link voltage, whereas the output waveform can be shaped by varying the buck duty cycle, D_{bk}. The AC-DC power decoupling is attained on the high voltage DC link and therefore requires a relatively low capacitance value. OCC control method was applied to shape the output voltage. OCC's fast response and low sensitivity to DC bus voltage ripple allowed applying yet smaller decoupling capacitor value, and has demonstrated low THD output for different types of highly non-linear loads.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2015.2457454, IEEE Transactions on Power Electronics

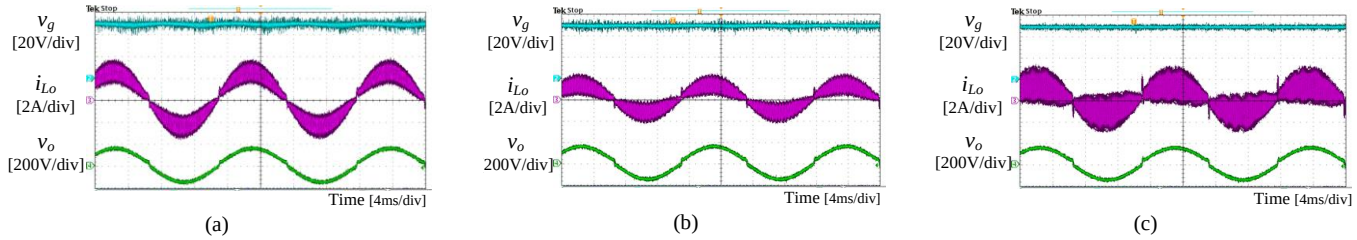


Fig. 14. Experimental results of v_g, i_{Lo} and v_o under different output power (V_g=48VDC): (a) 200W; (b) 100W; (c) 50W.

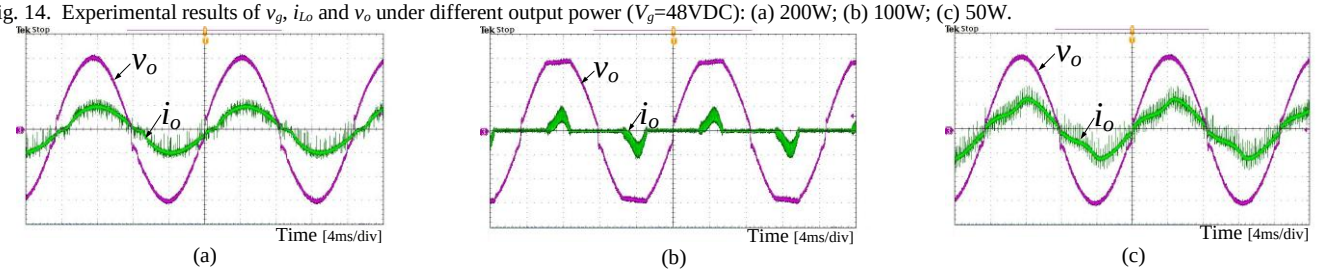


Fig. 15. Experimental results: SSBI's output voltage, v_o, and output current, i_o , under three different load conditions: (a) Linear RL load; (b) Non-linear load case I: Diode bridge with RC load; (c) Non-linear load case II: Resistor and saturable inductor load.

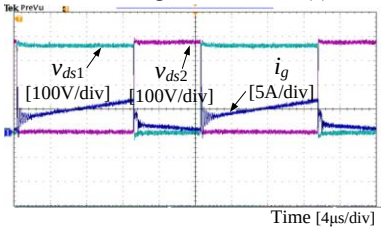


Fig. 16. Typical experimental waveforms of i_g, v_{ds1} and v_{ds2} during the switching cycle.

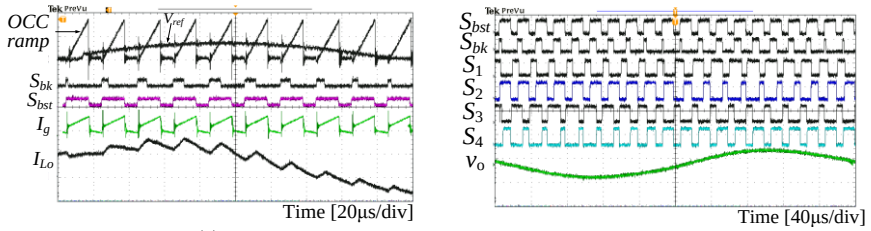


Fig. 17. Typical experimental waveforms (at reduced amplitude and frequency), where: (a) OCC ramp, V_{ref}, S_{bk}, S_{bst}, I_g and I_{Lo}; (b) switching functions S_{bk}, S_{bst}, $S_1 \ldots S_4$; and the output voltage v_o.

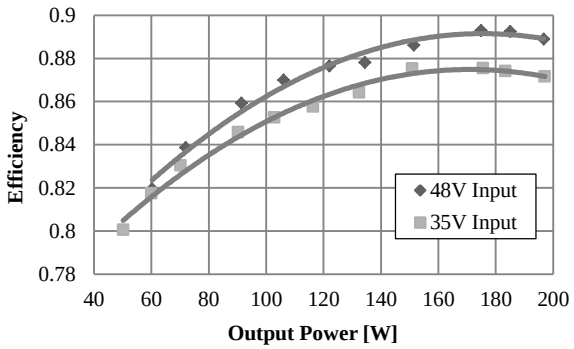


Fig. 18. Efficiency of experimental SSBI with 35/48 [V] input and 110VAC output.

REFERENCES

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Industry Application*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

[2] D. C. Martins and R. Demonti, "Interconnection of a photovoltaic panels array to a single-phase utility line from a static conversion system," in *Proc. IEEE PESC*, 2000, pp. 1207–1211.

[3] Q. Li and P. Wolfs, "A current fed two-inductor boost converter with an integrated magnetic structure and passive lossless snubbers for photovoltaic module integrated converter applications," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 309–321, Jan. 200.

[4] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "Power inverter topologies for photovoltaic modules-a review," in *Proc. IAS'02 Conf., vol. 2*, 2002, pp. 782–788.

[5] C. Vartak, A. Abramovitz, K. M. Smedley, "Analysis and Design of Energy Regenerative Snubber for Transformer Isolated Converters," *Power Electronics, IEEE Transactions on* , vol.29, no.11, pp.6030-6040, Nov. 2014.

[6] A. Abramovitz, Jia Yao, K. Smedley, "Derivation of a family of high step-up tapped inductor SEPIC converters," *Electronics Letters*, vol.50, no.22, pp.1626-1628.

[7] Jia Yao, A. Abramovitz, K. Smedley,"Analysis and design of charge pump assisted high step-up tapped inductor SEPIC converter with an "inductor-less" regenerative snubber," *IEEE Trans. on Power electron.*, vol. 30, Iss. 10, pp. 5565-5580, Oct.2015.

[8] A. Abramovitz, M. Heydari, Ben Zhao; K, Smedley, "Isolated flyback half-bridge OCC micro-inverter," *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE* , vol., no., pp. 2967-2971, 14-18 Sept. 2014.

[9] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[10] T. Shimizu, K. Wada, and N. Nakamura, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the DC input for an AC photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[11] S. B. Kjaer and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," in *Proc. IEEE Power Electron. Spec. Conf.*, 2003, pp. 1183–1190.

[12] Y. M. Chen and C. Y. Liao, "Three-port flyback-type single-phase micro-inverter with active power decoupling circuit," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2011, pp. 501–506.

[13] H. Hu, S. Harb, N. H. Kutkut, Z. J. Shen and I. Batarseh, "A Single-stage microinverter without using electrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2677–2687, Jun. 2013.

[14] H. Hu, S. Harb, X. Fang, D. Zhang, Q. Zhang, Z. J. Shen and I. Batarseh, "A three-port flyback for PV microinverter applications with power pulsation decoupling capability," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 3953–3964, Sep. 2012.

[15] R. O. Caceres and I. Barbi, "A boost DC-AC converter: analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, Jan. 1999.

[16] H. Ribeiro, F. Silva, S. Pinto and B. Borges, "Single stage inverter for PV applications with one cycle sampling technique in the MPPT

algorithm," in *Proc. 35th Annu. Conf. IEEE Ind. Electron.*, 2009, pp. 842–849.

[17] H. Ribeiro, A. Pinto and B. Borges, "Single-stage DC-AC converter for photovoltaic systems," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 604–610.

[18] T. Liang, J. Shyu, and J. Chen, "A novel DC/AC boost inverter," in *Proc. IEEE Energy Convers. Eng. Conf.*, 2002, pp. 629–634.

[19] C. Wang, "A novel single-stage full-bridge buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 150–159, Jan. 2004.

[20] N. Vazquez, L. Estrada, C. Hernandez and E. Rodriguez, "The tapped-inductor boost converter," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2007, pp. 531–538.

[21] J. P. Fohringer and F. A. Himmelstoss, "Analysis of a boost converter with tapped inductor and reduced voltage stress across the buffer capacitor," in *Proc. IEEE Int. Conf. Ind. Tech.*, 2006, pp. 126–131.

[22] K. M. Smedley, S. Cuk, "One-cycle control of switching converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 625–633, Nov. 1995.

[23] Y. Chen, K. M. Smedley, "A cost-effective single-stage inverter with maximum power point tracking," *IEEE Trans. Power Electron*., vol. 19, no. 5, pp. 1289-1294, Sep. 2004.

[24] R. W. Erickson, "The discontinuous conduction mode," in *Fundamentals of power electronics*, 2-nd ed. New York: Kluwer Academic, 2000, pp. 117–125.

[25] D. Meneses, F. Blaabjerg, O. Garcia, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic AC-module application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013.

[26] N. Kasa, H. Ogawa, T. Iida, and H. Iwamoto, "A transformer-less inverter using buck-boost type chopper circuit for photovoltaic power system," in Proc. IEEE Int. Conf. Power Electron. Drive Syst., 1999, pp. 653–658.

[27] S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking," *IEEE Trans.Power Electron.*, vol. 22, no. 5, pp. 1928–1940, Sep. 2007.

[28] M. Kusakawa, H. Nagayoshi, K. Kamisako, and K. Kurokawa, "Further improvement of a transformerless, voltage-boosting inverter for AC modules," *Solar Energy Mater. Solar Cells*, vol. 67, no. 1–4, pp. 379–387, Mar. 2001.

[29] H. Patel and V. Agarwal, "A single-stage single-phase transformer-less doubly grounded grid-connected PV interface," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 93–101, Mar. 2009.

[30] C. Yang, Y. Chang, C. Li, et al, "A module-integrated isolated solar micro-inverter," in *Proc. IEEE Int. Conf. Ind. Info.*, 2012, pp. 780–785.

[31] D. Cao, S. Jiang, F. Z. Peng, and Y. Li, "Low cost transformer isolated boost half-bridge micro-inverter for single-phase grid-connected photovoltaic system," in *Proc. IEEE Appl. Power Electron. Conf.*, 2012, pp. 71–78.

[32] B. Yang, Y. Zhao, and X. He, "Design and analysis of a grid-connected photovoltaic power system," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 992–1000, Apr. 2010.

[33] C. Pan, C. Lai, and M. Cheng, "A novel integrated single-phase inverter with auxiliary step-up circuit for low-voltage alternative energy source applications," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2234–2241, Sep. 2010.

[34] L. Kunzler, J. R. Tibola, M. L. da Silva Martins, and L. Schuch, "High efficiency AC photovoltaic module: efficiency or reduced number of components," in Proc. European Power Electro. Appl. Conf., 2013, pp. 1–10.