Improved Power Quality Bridgeless Converter Based SMPS for Arc Welding

Swati Narula, Bhim Singh, *Fellow, IEEE,* G. Bhuvaneswari, *Senior Member, IEEE,* Rahul Pandey

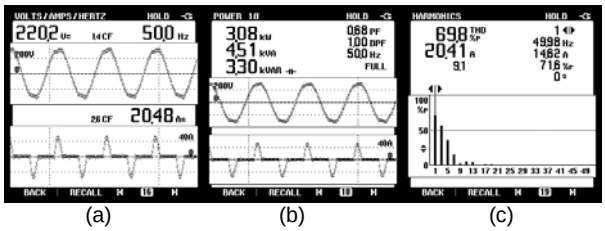
***Abstract*— This paper proposes a power factor corrected (PFC) bridgeless (BL) switched mode power supply (SMPS) for welding applications that possesses output voltage control and current limiting feature even during extreme overloading conditions at the output terminals. Eliminating input diode bridge rectifier minimizes conduction losses and improves thermal utilization of semiconductor devices. The front-end of proposed SMPS consists of a BL-boost converter operating in continuous conduction mode to attain unity power factor while at rear end, a PWM isolated full bridge DC-DC converter is used to regulate the output voltage. The design and implementation of this BL-arc welding power supply (AWPS) is presented showing its fast dynamic response to supply voltage and load variations. The performance of proposed AWPS is examined in terms of power factor, total harmonic distortion of the supply current, efficiency and output current limit over a wide range of line/load variations. Test results confirm effectiveness of proposed AWPS in maintaining an impeccable power quality at utility interface apart from achieving excellent output voltage regulation and current limiting capability.**

***Keywords*— Arc Welding Power Supply, Boost Converter, Bridgeless, Power Quality, Total Harmonic Distortion.**

I. INTRODUCTION

ARC welding is the most widely used and efficient welding process in many industries. So, it is essential to develop a simple, economical and energy efficient AWPS with reduced input current harmonics and high power factor (PF). Usually, a conventional full-bridge (FB) inverter based AWPS employs a diode bridge rectifier (DBR) at the point of common coupling (PCC) followed by a bulky DC-link capacitor [1-2]. The presence of a DBR with a large DC-link capacitor contributes to a peaky input current with a high total harmonic distortion (THD), low PF and deterioration of the system performance as shown in Fig. 1. The PF and current THD at the PCC for a conventional AWPS are 0.68 and 69.8% respectively which are not acceptable by the international power quality (PQ) standards [3-4]. In an effort to comply with the stringent restrictions posed by the international PQ standards, several PFC circuit based topologies are reported in the literature in which the DBR is followed by one of the PFC converters [5-7]. Designing a topology with high efficiency and over-current handling capability are the special requirements for an AWPS.

Boost converter based AWPS has been explored by Casanueva et al. [8] to attain PF correction at the input AC mains. DBR, being a rich source of harmonics, is unfit to be used in any application such as welding, where stringent international PQ standard norms are to be followed. It has also been observed from the existing literature that so far a BL converter based AWPS has not been investigated by the researchers. An effort has been made in this paper to reduce the input current harmonics and to attain a high PF at the PCC by using a BL converter at the front end of the AWPS. With tremendous developments in power electronics technology, it has now become possible to eliminate the DBR either partially or completely at the front end of an SMPS, by making use of BL-PFC converters. Several BL converter topologies have been reported in the literature [9-20] for PQ improvement. In BL topologies, there are only two semiconductor devices in the conduction path instead of three which is the case with DBR based PFC converters, resulting in considerable reduction in the conduction losses. Moreover, it also improves thermal utilization of the semiconductor switches as the rms current is bifurcated into two switches. Mitchell [13] has proposed a BL boost converter which eliminates the DBR completely from the input side. However, during the negative half cycle of the supply voltage, output ground has high frequency pulsating voltages. Therefore, eliminating the DBR completely in a BL boost converter significantly increases the common mode EMI noise. This demands a significantly larger common mode choke to meet the EMC standards thereby increasing the system cost and reducing the power density [14]. To overcome this issue, Tollik et al. [15] have proposed a BL boost converter using a bidirectional switch. But, this circuit requires an additional gate drive transformer as the gate voltages of the two switches are different. This, in turn, increases the complexity of the driver circuit. Further, it requires sampling of inductor current which makes the detection circuit more complex. The totem-pole BL boost converter topology also requires an isolated gate drive transformer and a complex detection circuit to sample the inductor current [16]. Furthermore, in totem-pole arrangement, the body diode of the switches performs the function of fast recovery diodes. Usually, the reverse recovery time of the body diode is much longer than the fast recovery diodes resulting in a substantial reverse recovery loss. Therefore, the efficiency of the totem-pole BL boost converter is expected to be quite low. This can be compensated by making use of it only in discontinuous conduction mode (DCM) of operation for low power applications. At higher power levels, the device stress issues associated with the DCM become exacerbated. Similarly, pseudo totem-pole BL boost converter also



(a) (b) (c)

Fig.1. Recorded PQ indices of AWPS (with DBR) at rated load with supply voltage as 220V; (a) Input voltage and current; (b) Input power and PF; (c) Harmonic spectrum of input current.

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The authors are with the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi 110016, India (e-mail: swatinarula.iitd@gmail.com, bsingh@ee.iitd.ac.in, bhuvan@ee.iitd.ac.in and rahul.ele@gmail.com)

demands a complex control and detection circuit making it less attractive for practical implementation [17]. Jang et al. [18] have also recommended multiple winding, multi-core inductor based BL boost converter. The design and analysis of multiple winding and multi-core inductor still remain major complexity for this configuration. Moreover, it has been observed that its efficiency is considerably low as compared to the efficiency of a BL boost converter reported in [19-20] where EMI losses have been appreciably reduced by incorporating two additional slow recovery diodes. Li et al. [21] have also stated that on the basis of efficiency, only pseudo totem-pole BL boost converter [17] and BL boost converter [19-20] are worth being considered. Since the gate drive circuits of BL boost converter [19-20] are referenced to ground, they are less sensitive to noise and easier to realize in industrial applications. Further, the input boost inductors in this configuration, operate as a common mode (CM) filter which helps in attaining a higher CM EMI reduction. Moreover, same signal can be used to trigger both the switches. This adds simplicity to the control circuit. Likewise, usage of two inductors results in better thermal performance as compared to using a single inductor. From the above discussion, it can be concluded that the BL boost converter is capable of offering high efficiency with low EMI losses and a better thermal management which makes it suitable for high power industrial applications such as welding. The EMI analysis of the proposed BL-boost converter is presented in detail in the Appendix section.

In this paper, mitigation of the power quality issues associated with conventional AWPSs is investigated. Apart from improving the power quality at the utility interface, this work also concentrates on improving the weld bead quality by restricting the output current to a desired limit even during short circuit; the control scheme also successfully regulates the output voltage even during wide variations in load and supply voltage. So, the major contribution of this paper is two-fold: (i) input PQ improvement and loss reduction by using a BL-boost converter at the front end and (ii) voltage regulation and over current limiting at the output end by using FB converter. The focus is mainly on the design, evaluation and development of an AWPS which requires a constant DC voltage at the output. In an arc welding process, a wide span of welding load/supply voltage range is encountered and it is necessary to optimize welding action over this entire operating range. Besides, an efficient control on welding current is desired during overload conditions to improve the weld bead quality. Another requirement of AWPS is its fast dynamic response as the stability of an arc welding process depends mainly on the dynamic behaviour of SMPS [22].

The proposed AWPS has a two-stage structure: the first stage is a PFC BL converter for harmonics mitigation which is followed by an isolated DC-DC converter for output voltage control. The BL converter operates in continuous conduction mode (CCM) which reduces the switch stress considerably even at high power levels. The input inductor helps in achieving perfect input current shaping and facilitates easy implementation of current mode control. The FB buck converter at second stage regulates DC output voltage and offers isolation by making use of a high frequency transformer (HFT) to ensure safe operation [23]. This configuration has advantages of improved input PQ, output voltage regulation for a wide range of line/load and over-current handling capability under extreme overload circuit conditions. The hardware implementation of proposed BL boost converter based AWPS has been carried out to validate its design and control configuration. Its performance has been evaluated over a wide range of load and supply voltage variations. Test results confirm an excellent performance of proposed AWPS.

II. Proposed BL Converter Based AWPS

A schematic diagram of proposed AWPS is shown in Fig. 2. The first stage consists of a PFC BL boost converter which converts an input AC voltage into an intermediate regulated DC voltage. The BL boost converter of proposed AWPS is formed by connecting two boost converters in such a way that each functions over a half-cycle period of supply voltage.

During the positive half-cycle, switch S_p, inductor L_p, diodes D_{p1} and D_{p2} conduct to deliver power from the source to the DC-link capacitor, C_d. Likewise, during the negative half cycle, switch S_n, inductor L_n, diodes D_{n1} and D_{n2} are in conduction. The input inductors L_p and L_n are designed to operate in CCM making the current through the input inductors remain continuous during the switching period. The boost converter utilizes a common DC-link capacitor C_d during both the half cycles of the supply voltage.

The second stage consists of an isolated FB buck converter to maintain a desired DC output voltage. The FB buck DC-DC converter has four switches (S_1, S_2, S_3 and S_4), HFT with its secondary center-tapped, a half-wave rectifier and a L_o-C_o filter at output to reduce output voltage ripple. Three identical FB converters are connected in parallel. The modular arrangement of FB converters offers several benefits such as ease of power expandability, use of power devices with comparatively low voltage and current ratings, easy maintenance etc.

III. Operation of Proposed AWPS

The proposed AWPS consists of a BL boost converter and FB buck DC-DC converters. The operation of both converters in one switching cycle is explained as follows.

A. Operating Modes of BL Boost Converter

For a BL boost converter operating in CCM, there are two intermediate operating stages for every PWM switching cycle. Fig. 3 shows the operating modes of BL boost converter for positive and negative half cycles of the supply voltage. Due to the symmetry of the BL converter topology, if its operation during one half-cycle of AC mains is analyzed, other half-cycle operation can easily be inferred. For analysis, all semiconductor devices are assumed to be ideal. Operating modes for the positive half-cycle are described as follows.

Mode I: This mode begins when switch S_p is turned on. The supply voltage v_s appears across the input inductor L_p, making its current to increase. The slow recovery diode D_{p1} completes the current conduction path as shown in Fig. 3(a). The DC-link capacitor C_d delivers energy to the isolated FB converter connected to load. Since no energy is supplied to the capacitor C_d during this mode, the output voltage V_d starts decreasing.

Mode II: Referring to Fig. 3(b), when switch S_p is turned off and diode D_{p2} becomes forward biased, an inductor, L_p transfers its stored energy to DC-link capacitor and the load. It

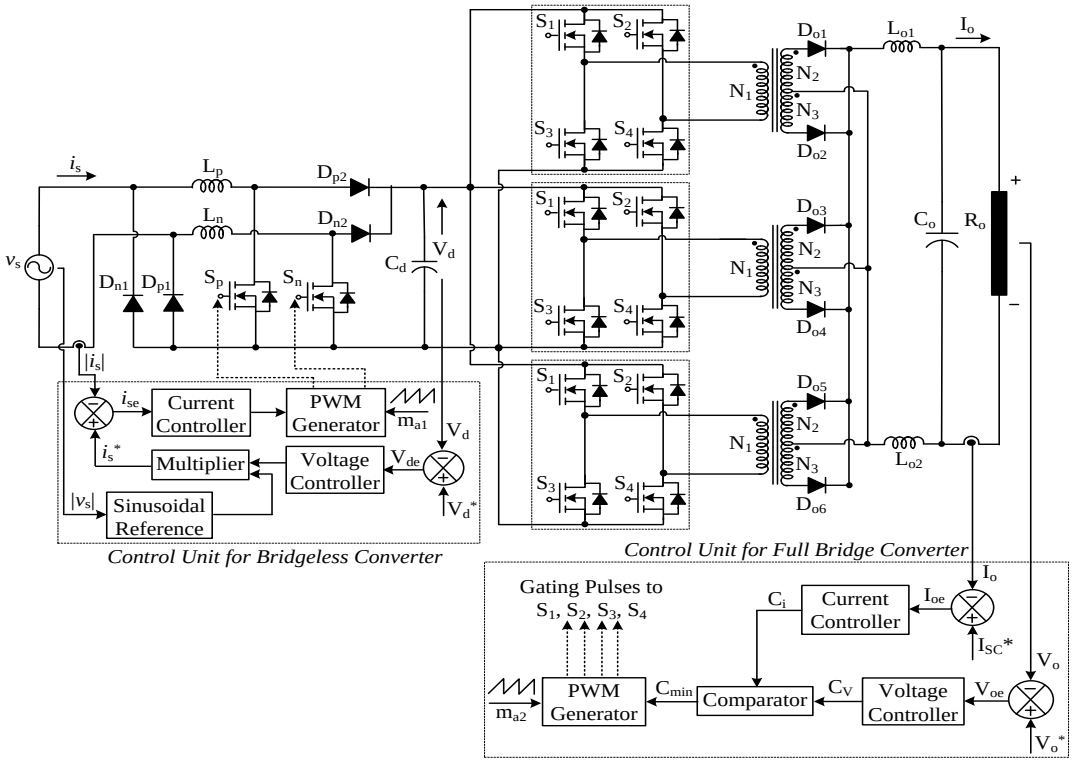

Fig.2. Schematic of BL boost converter and isolated FB converter based AWPS.

decreases the inductor current i_{Lp}. This stage continues until switch S_p is triggered again. Likewise, BL converter operates in negative half cycle as shown in Figs. 3(c-d).

B. Operating Modes of FB Buck Converter

For an isolated FB buck converter, the switching pairs of S_1-S_4 and S_2-S_3 are turned on alternately during each switching cycle. Four operating stages of FB buck converter in one switching cycle are as follows.

Mode I: Referring to Fig. 4(a), switches S_1 and S_4 are turned on, thus the DC-link voltage V_d, is applied across the primary winding of the HFTs having N_1 turns. Diodes D_{o1}, D_{o3} and D_{o5} become forward biased and the energy is stored in the output inductors L_{o1} and L_{o2}. The output inductor current starts increasing linearly and output filter capacitor C_o discharges through the welding load.

Mode II: The converter enters this mode when all the power switches are turned off as shown in Fig. 4(b). All the output diodes (D_{o1}, D_{o2}, D_{o3}, D_{o4}, D_{o5} and D_{o6}) conduct to freewheel the energy stored in the output inductors L_{o1} and L_{o2}. The current in the output inductor decreases linearly and energy is transferred to the output capacitor and welding load.

Mode III: This mode is similar to Mode I except that, switch pair S_2-S_3 conducts and diodes D_{o2}, D_{o4} and D_{o6} become forward biased while diodes D_{o1}, D_{o3} and D_{o5} remain open during this interval. The current flows through HFT and output inductors as shown in Fig. 4(c). The output inductors store energy and hence current starts increasing. The output capacitor C_o discharges through the welding load.

Mode IV: Likewise, modes II and IV are similar as shown in Fig. 4(d). When both the switching pairs are switched off, then the output rectifier diodes act as freewheeling diodes. The output inductors release the stored energy charging the output capacitor C_o. The operating modes repeat and switches trigger alternately in each switching cycle.

IV. Design of Proposed BL Converter Based AWPS

In this section, the design of a BL converter based AWPS is given in detail. In order to derive the necessary component design, the supply voltage, v_s is assumed to be constant as the switching frequency is much higher than the line frequency.

A. Design of BL Boost Converter

For the sake of simplicity, only one boost converter that operates in positive half-cycle of the supply voltage is being considered for analysis. The BL boost converter is designed for a DC-link voltage V_d of 360V.

1) Design of input inductors (L_p and L_n)

The input inductors of BL boost converter operate in CCM; so, the input current remains continuous throughout the entire switching period. The time interval t_{on}, during which the switch S_p conducts, is given as,

$$t_{on} = \frac{L_p \Delta I_{Lp}}{|v_s|} \tag{1}$$

where ΔI_{Lp} is peak-to-peak ripple inductor current. Similarly, off-time interval, t_{off} is given as,

$$t_{off} = \frac{L_p \Delta I_{Lp}}{V_d - |v_s|} \tag{2}$$

The BL-boost converter is operating at a fixed switching frequency, f_b of 45 kHz.

$$f_b = \frac{1}{t_{on} + t_{off}} = \frac{(V_d - |v_s|)|v_s|}{L_p \Delta I_{Lp} V_d} \tag{3}$$

The peak-to-peak ripple inductor current, ΔI_{Lp} is written as,

$$\Delta I_{Lp} = \frac{(V_d - |v_s|)|v_s|}{f_b L_p V_d} \tag{4}$$

From the above relation, the maximum ripple inductor current

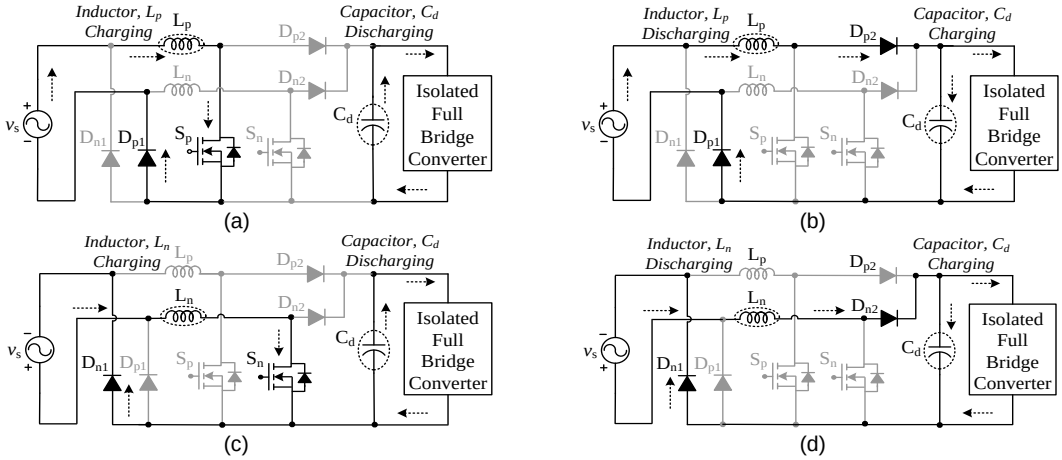

Fig.3. Operation of the steady state BL boost converter during positive (a-b) and negative half-cycle (c-d) of the supply voltage. (a) Mode I and (b) Mode II during positive half cycle; (c) Mode I and (d) Mode II during negative half cycle

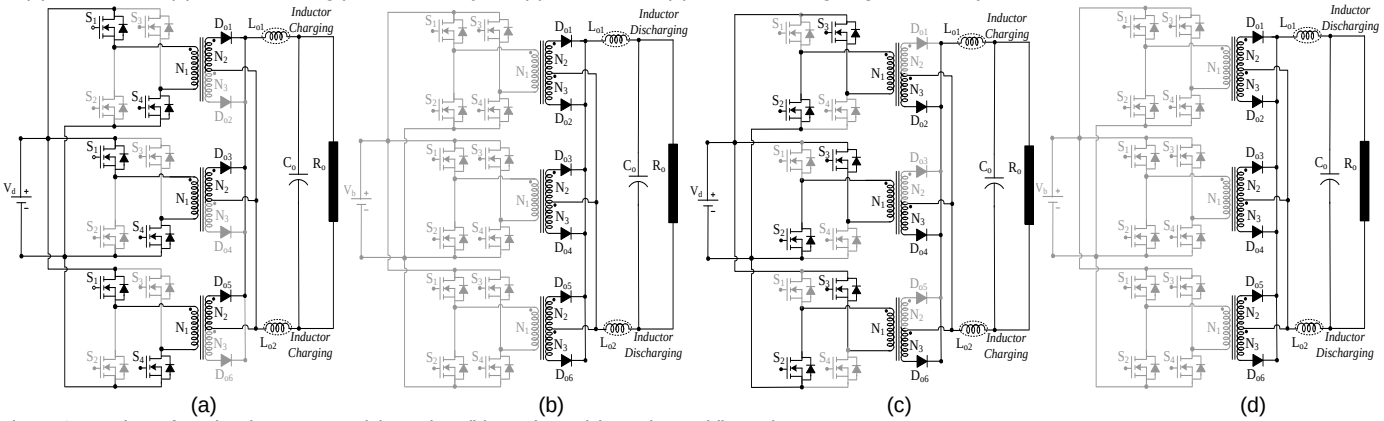

Fig.4. Operation of FB buck converter (a) Mode-I (b) Mode-II, (c) Mode-III, (d) Mode-IV.

appears at $|v_s| = V_b/2$. Hence, the maximum ripple inductor current is expressed as,

$$\Delta I_{Lpm} = \frac{V_d}{4 f_b L_p} \tag{5}$$

Moreover, to ensure CCM operation of boost converter, the maximum value of ripple current is calculated as,

$$\Delta I_{Lpm} = 0.25\sqrt{2} I_s = 0.25\sqrt{2}\,\frac{P_{in}}{V_s} = 0.25x\sqrt{2}x13.64 = 4.82 \text{ A} \tag{6}$$

Using (5) and (6), the value of input inductor is calculated as,

$$L_p = \frac{V_d}{4 f_b \Delta I_{Lpm}} = \frac{360}{4x45000x4.82} = 414.9\ \mu\text{H} \tag{7}$$

In order to ensure CCM operation of the input boost inductors, the value of L_p (and L_n) is selected to be 500 µH.

2) Design of DC-Link Capacitor (C_d)

The capacitor, C_d is designed such that it essentially delivers energy to the load during the switch on-time and also filters out the output voltage ripple.

$$C_d \geq \frac{P_o}{2\pi f_L V_d \Delta V_d} \geq \frac{3000}{2x\pi x50x360x36} \geq 736.8\ \mu\text{F} \tag{8}$$

where f_L is the line frequency i.e. 50 Hz and ΔV_d is the output voltage ripple which is considered to be 10% of the output voltage. The selected value of DC-link capacitor, C_d is 990 µF.

B. Design of FB Buck Converter

The output of BL boost converter acts as the input to the isolated FB buck converter operating at a switching frequency of 100 kHz. The second stage is made up of FB converters which are connected in modular arrangement, i.e., the three FB converters of less power rating connected in parallel to increase the overall power rating. Moreover, all the three HFTs are completely similar.

1) Design of Turns Ratio of HFT

For an isolated FB converter, the output to input voltage ratio can be expressed as,

$$\left\{V_d\left(\frac{N_2}{N_1}\right) - V_o\right\}\left(\frac{t_{on}}{T_s}\right) - \left\{V_o\left(\frac{t_{off}}{T_s}\right)\right\} = 0 \tag{9}$$

where $T_s = 1/f_s$ represents the switching period of FB buck converter. Thus the duty ratio D_f is given as,

$$D_f = \frac{V_o}{2V_d}\left(\frac{N_2}{N_1}\right) \tag{10}$$

Taking $D_f = 0.4$, the turns ratio is 4.8.

2) Design of Output Inductors (L_{o1} and L_{o2})

The output inductor is designed to operate in CCM. If the permissible ripple current is Δi_{Lo} (10% of I_o), then the value of output inductors ($L_{o1} = L_{o2}$) can be estimated as,

$$L_{o1} = \frac{V_o(0.5 - D_f)}{f_s(\Delta i_{Lo1})} = \frac{60x(0.5\text{-}0.4)}{100000x5} = 12\ \mu\text{H} \tag{11}$$

To ensure CCM operation of the inductor, the selected value of L_o is considered as 15 µH.

3) Design of Output capacitor (C_o)

The output capacitor C_o is designed to suppress output

voltage ripple. The voltage ripple on output capacitor C_o is as,

$$\Delta V_o = \frac{V_o(1-2D_f)}{32\, f_s^{\,2} L_{o1} C_o} \tag{12}$$

Thus, the output capacitor value is estimated for a given voltage ripple as,

$$C_o = \frac{V_o(1-D_f)}{8 f_s^{\,2} L_{o1}(\Delta V_o)} = \frac{60x(1-0.4)}{8x100000^2 x15x10^{-6}x6} \cong 5\ \mu F \tag{13}$$

The design values of the components used in the experimental AWPS are tabulated in Table I and the detailed specifications of the proposed AWPS is summarized in Table II.

TABLE I
DESIGN PARAMETERS FOR BL BOOST CONVERTER BASED AWPS

Component		Calculated Value	Experimental Value
BL Boost Converter	Inductors, L_p and L_n (APH33P60)	435.6 µH	500 µH
	Capacitor, C_d (KMR38d068)	736.8 µF	990 µF
FB Buck Converter	Turns Ratio, N_1/N_2 (EER43x15)	4.8	5
	Inductors, L_{o1} and L_{o2} (MP4010)	12 µH	15 µH
	Capacitor, C_o	5 µF	7 µF

TABLE II
SPECIFICATIONS FOR BL BOOST CONVERTER BASED AWPS

Input Power, P_{in}	3 kW
Supply voltage, V_s @ 50Hz	220 V
Switching frequency of BL boost converter	45 kHz
DC-link voltage, V_d	360 V
Switching frequency of FB buck converter	100 kHz
Permissible ripple in output voltage and current	10%
Output DC voltage	60 V

V. CONTROL OF PROPOSED AWPS

The control loops for BL boost converter and FB buck converter are designed individually. The average current mode control is used to attain CCM operation in BL boost converter while dual loop control scheme is employed for FB buck converter. For the BL boost PFC converter, the zero crossing detection (ZCD) method is utilized to sense the supply voltage. The ZCD circuit comprises of diode-OR circuit that makes the sensing of supply voltage during both the half cycles possible. Moreover, switching losses are minimized by using ZCD technique.

A. Control of BL Boost Converter

The BL boost converter operates in CCM using average current mode control thus offering the advantage of input current shaping and PF correction. The DC-link voltage, V_d is sensed and then compared with the reference voltage, V_d^*. The voltage error, V_{de} at any n^{th} instant is expressed as,

$$V_{de}(n) = V_d^*(n) - V_d(n) \tag{14}$$

This voltage error signal is processed by a proportional-integral (PI) controller to generate an output V_{cv}.

$$V_{cv}(n) = V_{cv}(n-1) + k_{pv}\{V_{de}(n) - V_{de}(n-1)\} + k_{iv} V_{de}(n) \tag{15}$$

where k_{pv} and k_{iv} denote the proportional and integral gains of the PI voltage controller respectively. The feed-forward voltage comes from the rectified AC mains voltage. The reference input current i_s^* is generated as the product of the PI controller output and the unit template of the supply voltage acting as a sinusoidal reference.

$$i_s^*(n) = \left|\frac{v_s(n)}{V_{sm}}\right| V_{cv}(n) \tag{16}$$

where V_{sm} is the peak amplitude of the supply voltage and $\left|\frac{v_s(n)}{V_{sm}}\right|$ is the unit template of the supply voltage.

The error between the reference input current and sensed input current is expressed as,

$$i_{se}(n) = i_s^*(n) - i_s(n) \tag{17}$$

The current error is then processed by another PI controller and the output of the current controller is given as,

$$V_{ci}(n) = V_{ci}(n-1) + k_{pi}\{i_{se}(n) - i_{se}(n-1)\} + k_{ii} i_{se}(n) \tag{18}$$

where k_{pi} and k_{ii} refer to the proportional and integral gains of the PI current controller respectively. At last, the current controller output is then compared with a high frequency saw-tooth waveform m_{a1} to generate the gating pulses for the BL boost converter.

$$\begin{aligned} &\text{For } v_s > 0;\ \left\{\begin{matrix}\text{If } m_{a1}(t) < V_{ci}(t), \text{ then } S_p = 1\\ \text{If } m_{a1}(t) \geq V_{ci}(t), \text{ then } S_p = 0\end{matrix}\right\}\\ &\text{For } v_s < 0;\ \left\{\begin{matrix}\text{If } m_{a1}(t) < V_{ci}(t), \text{ then } S_n = 1\\ \text{If } m_{a1}(t) \geq V_{ci}(t), \text{ then } S_n = 0\end{matrix}\right\}\end{aligned} \tag{19}$$

where '1' represents the on state and '0' refers to the off state of power switches S_p and S_n.

B. Control of FB Buck Converter

In order to regulate the output voltage and to ensure good weld bead quality even during over-load conditions, dual loop control scheme is adopted for FB buck converter. The error voltage, V_{oe} between the sensed output voltage V_o and reference voltage V_o^* is given to another PI voltage controller. The output of the PI voltage controller is expressed as,

$$C_V(k) = C_V(k-1) + k'_{pv}\{V_{oe}(k) - V_{oe}(k-1)\} + k'_{iv} V_{oe}(k) \tag{20}$$

where k'_{pv} and k'_{iv} are proportional and integral gain constants of the voltage controller respectively.

Concurrently, the output current I_o is taken as a feedback signal and compared with the output current limit I_{SC}. The generated current error is given to a PI current controller to restrict the output current within the desired limits.

$$C_i(k) = C_i(k-1) + k'_{pi}\{I_e(k) - I_e(k-1)\} + k'_{ii} I_e(k) \tag{21}$$

where k'_{pi} and k'_{ii} represent proportional and integral gain constants of current controller respectively. Thereafter, a comparator compares the outputs of both PI controllers (C_V and C_i) and whichever is lower is given to the PWM generator to generate the gating pulses. The PWM duty cycle is adjusted in accordance with the changes required in the output DC voltage and the welding current.

VI. HARDWARE IMPLEMENTATION OF PROPOSED AWPS

To validate the operating principle and viability of the proposed AWPS, a prototype is designed and built, using the specifications listed in Table II. A Piccolo based on TI-TMS320F28027 (12 ADC bits) having a sampling frequency of 20µs is employed for the control of the proposed AWPS. Test results are recorded and discussed to evaluate the

performance of proposed AWPS in the following subsections.

A. Steady State Performance

Fig. 5(a) illustrates the steady state performance of the proposed AWPS at rated load and at 220 V supply voltage showing the supply voltage (v_s), supply current (i_s), output voltage (V_o) and output current (I_o). The input current is sinusoidal and in phase with the supply voltage. The intermediate results having BL boost converter DC-link voltage (V_d) and current (I_d) are shown in Fig. 5(b). The controller regulates the output voltage, V_o at 60V while the DC-link voltage, V_d is maintained at 360V. The BL operation of the front end converter is clearly visible in Fig. 5(c). It can be seen that switch S_p conducts in the positive half cycle of the supply voltage while switch S_n conducts during the negative half cycle. Furthermore, the peak switch stress (V_{Sp} and V_{Sn}) is observed to be 360 V. Fig. 5(d) presents the boost inductor current waveforms to illustrate the CCM operation of the boost inductors L_p and L_n. It can be perceived from Fig. 5(d) that inductor L_p operates in positive half cycle while inductor L_n functions during negative half cycle of the supply voltage.

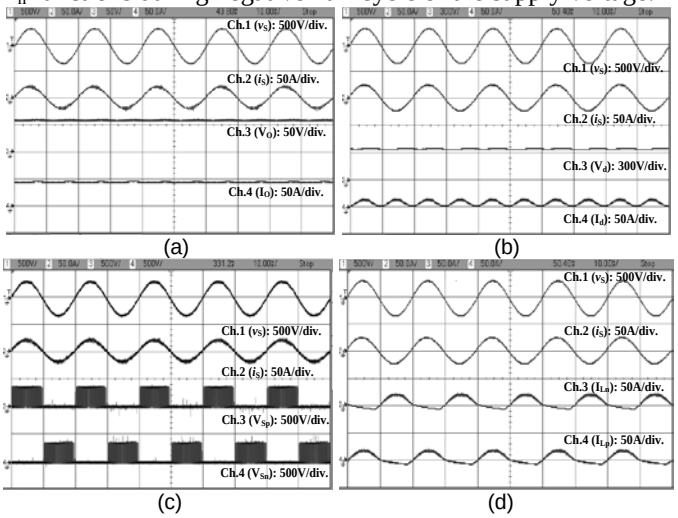

Fig.5. Steady state performance of proposed converter at rated load and 220V (rms) supply voltage. (a) Waveforms of v_s, i_s, V_o and I_o; (b) Waveforms of v_s, i_s, V_d and I_d; (c) Waveforms of BL converter switch voltage stress S_p and S_n; (d) Waveforms of v_s, i_s, I_{Ln} and I_{Lp}.

B. Dynamic Performance under Supply Voltage Variations

Apart from steady state performance, performance of proposed power supply is also studied at varying supply voltages and loads. To illustrate the efficacy of proposed AWPS under supply voltage variations, the supply voltage is varied from 183V (rms) to 256V (rms) as shown in Figs. 6(a-b) and 6(c-d) respectively. Even on varying the supply voltage, the converter draws almost the same rated power thus no change in the output voltage and output current is observed. Moreover, the BL boost converter controller enforces the input current to follow the supply voltage throughout the wide range of supply voltage.

C. Dynamic Performance under Light Load

The stability of an AWPS mainly relies on its dynamic performance, thus it is essential to analyze the dynamic behavior under light load condition. In Fig. 7(a), the load is suddenly varied from rated to light load (approx. 16% of rated load) conditions. It depicts that the controller efficiently maintains a constant output voltage (V_o = 60V) with the load current decreasing to 6.58 A. The input current remains in phase with the supply voltage and the PF remains close to unity throughout the widely varying load range.

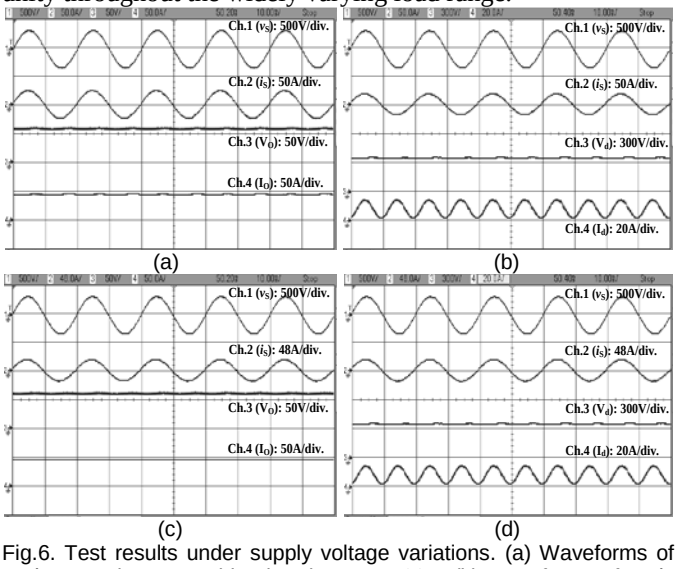

Fig.6. Test results under supply voltage variations. (a) Waveforms of v_s, i_s, V_o and I_o at rated load and at v_s = 183V; (b) Waveforms of v_s, i_s, V_d and I_d at rated load and at v_s = 183V; (c) Waveforms of v_s, i_s, V_o and I_o at rated load and at v_s = 256V; (d) Waveforms of v_s, i_s, V_d and I_d at rated load and at v_s = 256V.

D. Dynamic Performance under Over Load

During arc welding process, the converter quite frequently functions with huge variations in the load. This causes several problems such as spattering, poor weld bead quality, instability of arc length, etc. The performance of the proposed AWPS under overload conditions is shown in Fig. 7(b). The maximum output current limit (I_{sc}) for the proposed topology is set at 50A, which can be altered accordingly as per the requirement while designing the controller. Therefore, whenever the load is increased beyond a certain limit such that the output current becomes greater than 50A the controller switches from constant voltage to constant current and successfully maintains constant current at the output. It is evident from the test results that the dual loop controller limits the output current to 50A even during overload conditions while the output voltage is reduced (i.e., C_i becomes less than C_v). So, the duty cycle of the switches now completely depends upon the value of C_i instead of C_v. By controlling the output current during overload conditions, one can substantially improve the weld bead quality.

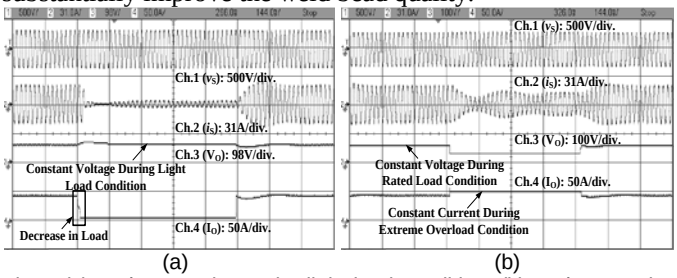

Fig.7. (a) v_s, i_s, V_o and I_o under light load condition; (b) v_s, i_s, V_o and I_o under overload condition.

E. Improved PQ of Proposed AWPS

The performance of proposed BL converter based AWPS at different power levels, is tabulated in Table III. It can be perceived that even at low power levels the efficiency of the proposed AWPS is greater than 80%. Moreover, the PF and DPF remain close to unity at the observed power levels. The

performance parameters such as active power (P), reactive power (Q), apparent power (S), supply voltage (v_s), supply current (i_s) and the impacts of load and supply voltage variations on various PQ indices such as PF, DPF, DF and THD are shown in Fig. 8. THD and PF of supply current at input AC mains are the most important PQ indices to be evaluated as their deterioration affects the longevity and efficiency of the equipment. These test results significantly corroborate the improved PQ operation of proposed AWPS. It can be clearly seen that the PF is approaching unity and the THD of AC current is within limits specified by IEC61000-3-2 standard thus improving PQ at input AC mains.

TABLE III
PERFORMANCE OF PROPOSED AWPS AT DIFFERENT POWER LEVELS

Input Power, P_{in} (kW)	Output Power, P_o (kW)	Efficiency, η (%)	THD of I_s (%)	I_s (A)	PF	DPF
0.490	0.401	81.83	12.3	2.266	0.96	0.98
1.01	0.892	88.32	7.7	4.516	0.99	1.0
1.52	1.38	90.79	5.0	7.02	0.99	1.0
1.99	1.83	91.96	3.8	8.96	1.0	1.0
2.49	2.29	91.97	3.1	11.42	1.0	1.0
3.07	2.80	91.21	2.7	13.93	1.0	1.0

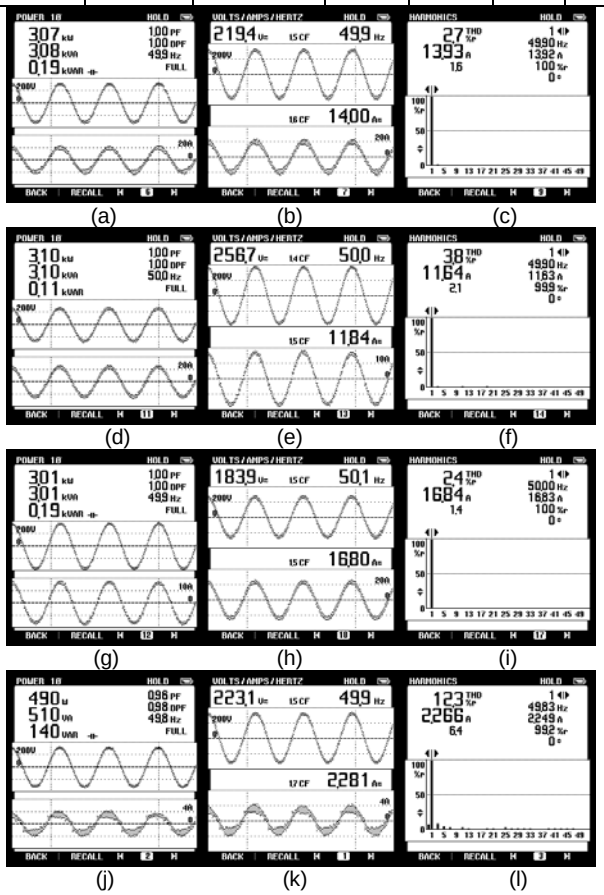

Fig.8. PQ indices of proposed BL boost converter based AWPS; (a)–(c) at rated load and v_s=220 V, (d)–(f) at rated load and v_s =256V, (g)–(i) at rated load and v_s=183V (j)–(l) at light load and v_s =220 V.

F. Comparative Analysis with Different Configurations

In Table-IV, a brief comparison of proposed BL boost configuration with other BL converter topologies [10, 13, 11, 24, 25] is shown. As compared to the other BL buck-boost converters, the proposed converter utilizes the least number of components and has minimum number of components in the current conduction path thereby reducing the system cost and losses. Besides, its PFC capability is far better than the BL-buck converter. Moreover, the BL-boost converter [13] suffers from the drawback of excessive EMI emission. Thus the proposed BL boost converter is considered as workable solution as PFC converter for AWPS.

The performance of proposed BL boost converter based AWPS is also compared with (i) boost converter based AWPS which is having DBR followed by boost converter as front end PFC converter and (ii) conventional AWPS which comprises of only DBR FB buck converter. Fig. 9(a) shows THD of supply current with input power for conventional, simple boost and proposed BL boost converter based AWPS.

TABLE IV
COMPARATIVE ANALYSIS OF PROPOSED BL BOOST CONVERTER WITH EXISTING BL CONFIGURATIONS

Configuration	Components					Devices conducting in ½ cycle
	S_w	D	L	C	Total	
BL-Buck [10]	2	4	2	2	10	5
BL-Boost [13]	2	2	2	1	7	5
BL-Buck Boost [11]	3	4	1	3	11	8
BL-Cuk [24]	2	3	3	3	11	7
BL-SEPIC[25]	2	3	3	3	11	7
Proposed BL Boost	2	4	2	1	9	5

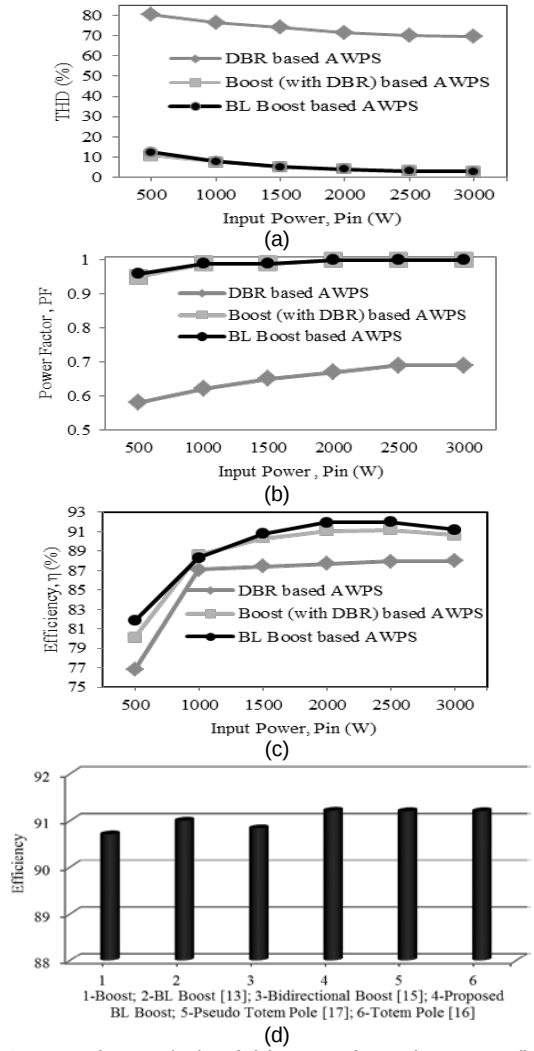

Fig.9. Comparative analysis of (a) THD of supply current (b) PF (c) efficiency for the conventional, boost (with DBR) and proposed BL converter based AWPS; (d) efficiency of different BL boost configurations.

It can be seen that the THD in case of conventional scheme varies from 80.6% to 69.8% which makes it violate the

international harmonic standards. In Fig. 9(b), the variation of PF with input power for all the three cases are shown in which the conventional scheme is found to be the worst. A comparison in terms of efficiency is depicted in Fig. 9(c). It can be seen that the overall losses associated with the proposed BL converter based AWPS is coming out to be the least as compared to the other two configurations. The comparison in terms of efficiency of different BL boost configurations is presented in Fig. 9(d). It should be noticed that the boost converter is not the highly efficient topology as compared to the BL topologies. Totem-pole boost [16], pseudo totem-pole [17] and proposed BL-boost converter have better efficiency. However, as already discussed in the introduction section, totem-pole boost [16] and pseudo totem-pole [17] are not usually preferred. Hence, the proposed BL boost converter based SMPS having the highest efficiency emerges out as a recommended solution for arc welding applications.

VII. Conclusion

A BL boost converter based AWPS has been designed and implemented to demonstrate its improved performance with regard to PQ at input AC mains. Considering wide range of load and supply voltage variations as it is seen realistically in a welding power supply, the complete analysis has been carried out and it is seen that the power supply performs exceedingly well in the entire operational range. The supply current THD is found to be well within the acceptable limits, with a PF close to unity which meets the stringent requirements of IEC 61000-3-2 standard. Moreover, the DC-link voltage is regulated to a constant value throughout the operating range. The quality of the weld in arc welding process is enhanced by providing the output voltage control along with the over-current handling capability. The proposed topology has also offered the advantage of improved thermal utilization, reduced conduction loss thus leading to a higher efficiency. Furthermore, it can be inferred from the obtained test results that the proposed BL converter based system has provided robustness and fast response. Altogether, the proposed welding power supply has shown satisfactory performance so that it could be a good solution for arc welding applications.

Appendix

In case of BL-boost converter; two boost converters are connected (back-to-back) resulting in a symmetrical circuit for both positive and negative half cycles of the supply voltage. Therefore, only positive half-cycle of the supply voltage is considered. Based on the symmetrical operation, the circuit during positive half cycle is shown in Fig. 10(a). Considering the output filter capacitor as a short circuit and boost inductor as an open circuit during high frequency operation, these two components can be ignored to simplify the circuit as illustrated in Fig. 10(b). Furthermore, the semiconductor components, such as fast recovery diode and MOSFET can be considered as a capacitor and pulse source respectively in high frequency domain. Fig. 10(c) depicts the equivalent circuit using Thevenin's theorem. Therefore, the proposed BL-boost converter during positive half cycle of the supply voltage is equivalent to a pulse voltage source V_{seq} in series with a capacitor C_{eq}, such as,

$$V_{seq} = -V_{ds} x \frac{C_{Sp}}{C_{eq}} \quad (22)$$

where, C_{Sp} and C_{Sn} are the parasitic capacitances of MOSFETs, C_b is the capacitance between output ground and the power earth. Usually, C_b is 10 to 20 times that of C_{Sp} and C_{Sn}. Therefore, if there is any voltage pulse across it, it causes a significant extra CM current flow through it leading to CM EMI problems. However, referring to Fig. 10(c), it is evident that C_b is connected directly between the source of the MOSFET and the earth. This results in no pulse voltage across C_b, leading to reduced CM current of the circuit. Likewise, for negative half cycle of the supply voltage,

$$V_{seq} = -V_{ds} x \frac{C_{Sn}}{C_{eq}} \quad (23)$$

Assuming $C_{Sp} = C_{Sn} = C_S$, the EMI model for the complete cycle of the supply voltage is given as,

$$V_{seq} = -V_{ds} x \frac{C_S}{C_{eq}} \quad (24)$$

$$I_{seq} = -V_{ds} x(\omega C_S) \quad (25)$$

It is observed that although the switching operation generates high frequency pulses inside the proposed BL-boost circuit, they do not impact the voltage waveform between power ground and neutral. Since, the power ground is connected to the neutral for the whole ac period via return diodes D_p and D_n, all the pulsed voltages go into the earth through the parasitic capacitance C_S of the MOSFETs. This in turn, gives a continuous and smooth waveform between power ground and the neutral. Furthermore, (25) depicts that the CM current flows through the parasitic capacitance of MOSFETs. With all these considerations, the EMI filter used for the proposed topology is illustrated in Fig. 11.

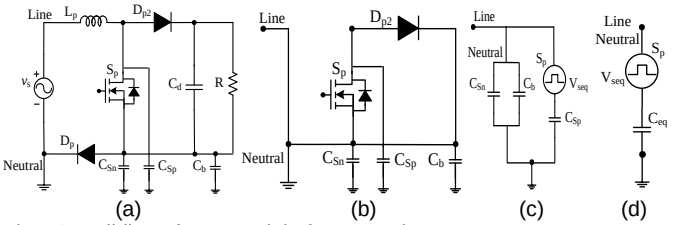

Fig. 10. Building of EMI model of proposed BL-Boost converter.

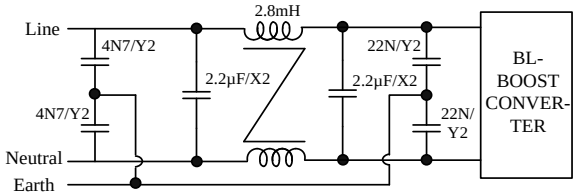

Fig. 11. EMI filter for the proposed BL-Boost converter based AWPS.

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Swati Narula received the B. Tech. degree in electrical & electronics engineering from GGSIP University, Delhi, in 2009. She has joined as MS(R) student in Department of Electrical Engg., IIT Delhi, New Delhi in 2010. She subsequently completed the PhD from Indian Institute of Technology Delhi, India in 2015. Her area of interest includes power electronics & switched-mode power supplies.

Bhim Singh (SM'99, F'10) received Bachelor of Engineering (Electrical) degree from University of Roorkee, Roorkee, India, in 1977, and M.Tech. (Power Apparatus and Systems) and Ph.D. degrees from Indian Institute of Technology (IIT), New Delhi, India, in 1979 and 1983, respectively. In 1983, he joined Department of Electrical Engineering, University of Roorkee, as a Lecturer. In December 1990, he joined Department of Electrical Engineering, IIT Delhi, New Delhi, India, as an Assistant Professor, where he has became an Associate Professor in 1994 and a Professor in 1997.

Prof. Singh is a Fellow of the Indian National Academy of Engineering (INAE), the National Science Academy (NSc), the Indian Academy of science (IASc), the Institute of Engineering and Technology (IET), the Institution of Engineers (India) (IE(I)), and the Institution of Electronics and Telecommunication Engineers (IETE).

G. Bhuvaneswari (SM'99) obtained her Bachelor's degree from College of Engineering, Madras in 1985 and M.Tech. and Ph.D. degrees from IIT, Madras, India. She was working as a faculty in College of Engineering Madras right after her Ph.D. after which she was working for ComEd, Chicago, IL. She has been a faculty member in the Dept. of Elec. Engg, IIT Delhi since 1997. She is a Fellow of IET-UK, IE(I), IETE and INAE. Her areas of interest are Power Electronics and its application areas like Drives, Power conditioning, Power Quality, Power Supplies, Renewable Energy, HVDC and FACTS.

Rahul Pandey received the B.Tech degree in electrical engineering from North Eastern Regional Institute of Science and Technology, Itanagar, India, in 2003 and M.Tech degree in electrical engineering from Indian Institute of Technology, New Delhi, India in 2007. He is currently working towards the Ph.D. degree in the Department of Electrical Engineering, Indian Institute of Technology, Delhi, New Delhi, India. His areas of research interests include power electronics, power quality, and digital control.