This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2016.2543506, IEEE Transactions on Power Electronics

Design and Steady State Analysis of Parallel Resonant DC-DC Converter for High Voltage Power Generator

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Abstract

Abstract –A novel voltage-doubling circuit with parallel resonant DC-DC converter is proposed. The converter consists of full-bridge inverter, resonant tank, high frequency high voltage transformer, and voltage-doubling circuit. In the high voltage applications, low output voltage ripple has been given much attention. The output voltage step-up ratio is increased by two parts. One is a high frequency high voltage transformer and the other is a voltage-doubling circuit. The novel voltage-doubling circuit can not only reach a higher output voltage but also reduce output ripple to a lower level than the conventional one. Therefore, while maintaining the same output voltage, the transformer's turn ratio can be reduced compared with the conventional voltage-doubling circuit. The output power can be adjusted by the phase-shift control technique. In addition, combining this technique with the parallel resonant tank can make all the switches achieve zero voltage turn on (ZVS). The operating principles, steady-state analysis, and the parameter designs are discussed in this paper. Finally, a prototype circuit with 400V input voltage, 40kV output voltage, and 300W output power is developed in the laboratory to verify the performance of the proposed converter.

Index Terms –voltage-doubling circuit, steady-state analysis, design parameters

I. INTRODUCTION

In recent years, high voltage DC power supplies are widely used in many applications, such as extraoral source X-ray system, plasma processing, electron beam Systems, etc[1-4]. In high voltage applications, it is important to reduce the output voltage ripple and increase output voltage. Therefore, the voltage-doubling circuit plays an important role. There are two basic topologies for voltage-doubling circuits: half wave voltage-doubling circuits and full wave voltage-doubling circuits. Different voltage-doubling circuits can significantly decide whether the output voltage ripple was reduced or not [5]. For example, in literature [6], the voltage-doubling circuit is suitable for high voltage application, but it also increases the output voltage ripple. Furthermore, the voltage stress of individual capacitor is different. In literature [7], the voltage-doubling circuit was also applied in high voltage applications, but it has a problem similar to the one in literature [6]. As usual, the individual capacitor has distinct voltage stress. In literature [8], the voltage-doubling circuit was a variant type, but it still can't effectively reduce the output voltage ripple. In literature [9,11], the output voltage ripple was effectively reduced, but the circuit needs more components. In this paper, a novel voltage-doubling circuit with parallel DC-DC converter is proposed. While the output voltage maintains the same as other structures do, the output voltage ripple is reduced significantly.

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The full-bridge DC-DC converter and phase-shift control technique are widely used in high voltage DC power supply. The adopted conventional full-bridge DC-DC converter usually doesn't contain resonant tanks. However, the voltage across the transformer's primary side will ring and cause the consumption of the power converter to increase and the stress of the circuit components to increase [12,13]. Two basic topologies of resonant circuits are commonly used in the full-bridge DC-DC converter, resonant circuits including the series resonant circuit and parallel resonant circuit [14-16]. Both of the topologies can make all the switches in the circuit achieve zero voltage switching (ZVS) or zero current switching (ZCS) [17-22]. Therefore, it can reduce the voltage or current stress of the switches and increase the whole efficiency of the converter. Normally, the DC-DC resonant converter can be examined in the time domain or in the frequency domain. It was straightforward for a DC-DC resonant converter to be analyzed by the frequency domain in most of the literature [23-25]. However, the equivalent circuit in frequency domain was ignored in the equivalent capacitor of the voltage-doubling circuit. The steady state analysis of the RC load was proposed in [26]. In this paper, the waveform of the voltage across the transformer's primary side and the waveform of the current flowing through the resonant capacitor parallel to the transformer are directly used for the purpose of analyzing the equivalent capacitor. This method is not only a good solution for steady state analysis of DC-DC resonant converter, but also an important examination on the resonant tank. However, it can't decide the output ripple and the capacitance of the voltage-doubling circuit. This paper not only solves the problem listed above but also decides

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the capacitance of the voltage-doubling circuit by using basic sinusoidal waveform analysis. Fig. 1 shows a novel voltage-doubling circuit with parallel resonant DC-DC converter proposed in this paper.

In this paper, a novel voltage-doubling circuit with parallel resonant DC-DC converter is proposed in Fig. 1. A novel voltage-doubling circuit can not only reach a higher output voltage but also reduce output ripple to a lower level than the conventional one. Therefore, while having the same voltage multiple levels as conventional ones, the proposed converter can have a smaller output voltage ripple. In addition, the output power can be adjusted by the phase-shift control technique. Using this technique with the parallel resonant tank can make all the switches achieve zero voltage turn on (ZVS). The analytical methodology is proposed and applied to the parallel resonant tank in order to discuss its steady state conditions. By using this method, the output ripple and equivalent capacitance of the voltage-doubling circuit was decided. Finally, a prototype circuit with 400V input voltage, 40kV output voltage and 300 W output power is developed and the performance of the proposed converter is verified.

II. Operating Principle of the Proposed Voltage-Doubling Circuit

In Fig. 1, the novel DC-DC converter circuit consists of power switches S_a-S_d, a resonant inductor L_r, a resonant capacitor C_r, a leakage inductor L_p, a high-frequency high- voltage transformer T_r, voltage-doubling capacitors C_1-C_{2n+1} and C_2-C_{2n}, rectifier diodes, and a high voltage load R_L. The voltage of v_{cr} corresponds to sinusoidal waveform when the inductor L_r and

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capacitor C_r are resonating. In order to simplify the analysis of the voltage-doubling circuit, the following conditions are assumed:

1). The voltage v_{Cr} could be approximated as a sinusoidal waveform.

2). All the capacitors and diodes are treated as ideal.

3). Capacitors C_1-C_{2n+1} and C_2-C_{2n} are large enough, and can be assumed as constant voltage sources.

Fig. 2 shows the key waveforms of the novel DC-DC converter circuit. There are eight stages in one switching period. The following description of each operating stage corresponds to a novel DC-DC converter circuit in Fig. 1.

1) Mode I [t_0-t_1]: During this time interval, the power switches S_a and S_d are turned on. The resonant inductor L_r and the resonant capacitor C_r are charged by the DC-source V_{in}, so the resonant inductor current i_{Lr} and the resonant capacitor voltage v_{Cr} both increases. Simutaneously, the capacitors C_3-C_{2n+1} release energy to the load and the output voltage V_o is decreased. The current-flow path is shown in Fig. 3(a). When the output voltage drops to $V_{o,min}$, this mode ends.

2) Mode II [t_1-t_2]: During this time interval, the power switches S_a and S_d maintain on. When $t = t_2$, the voltage v_{Cr} becomes higher than V_{Cr1} which makes the transformer T_r secondary side voltage sufficiently higher than the voltage capacitor C_1 , so the leakage inductor L_p releases energy to the load. Furthermore, the capacitors C_2-C_{2n} transfer energy to the capacitors C_1-C_{2n+1}. The

current-flow path is shown in Fig. 3(b). This mode ends when power switches S_a and S_d are turned off.

3) Mode III [t_2-t_3]: During this time interval, the resonant inductor current i_{Lr} begins to charge the parasitic capacitor of C_{ossa} and C_{ossd}, and discharge the parasitic capacitor of C_{ossb} and C_{ossc}, respectively. Then, the power switches S_b and S_c are achieving ZVS when the power switches S_b and S_c are turned on. The current-flow path is shown in Fig. 3(c). When the current i_p increases to $I_{p,max}$, this mode ends.

4) Mode IV [t_3-t_4]: During this time interval, the power switches S_b and S_c are turned on. The resonant capacitor C_r transferes energy to the resonant inductor L_r. Simultaneously, the leakage inductor L_p releases energy to the load. The current-flow path is shown in Fig. 3(d). When the output voltage V_o reaches $V_{o,max}$, this mode ends.

5) Mode V [t_4-t_5]: During this time interval, the power switches S_b and S_c maintain on. The resonant inductor L_r and the resonant capacitor C_r are charged by the DC-source V_{in}. Then, the capacitors C_3-C_{2n+1} release energy to the load. The current-flow path is shown in Fig. 3(e). When the voltage v_{Cr} reaches V_{cr2}, this mode ends.

6) Mode VI [t_5-t_6]: At $t = t_5$, the voltage v_{Cr} reaches V_{Cr2} which makes the transformer T_r secondary side voltage sufficiently higher than the voltage capacitor C_2, so the leakage inductor L_p releases energy to the load. Furthermore, the capacitors C_1-C_{2n+1} transfer energy to the capacitors C_2-C_{2n}. The current-flow path is shown in Fig. 3(f). When the current i_p recheas $-I_{p,max}$, this mode ends.

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7) Mode VII [t_6-t_7]: During this time interval, the power switches S_b and S_c are turned off. The resonant inductor current i_{Lr} begins to charge the parasitic capacitors of C_{ossb} and C_{ossc}, and discharge the parasitic capacitor of C_{ossa} and C_{ossd}, respectively. The power switches S_a and S_d are achieving ZVS when the power switches S_a and S_d are turned on. The current-flow path is shown in Fig. 3(g). When power switches S_b and S_c turned off, this mode ends.

8) Mode VIII [t_7-t_8]: During this time interval, the power switches S_a and S_d turned on. The output voltage V_o is dropping. The capacitors C_1-C_{2n+1} transfer energy to the capacitors C_2-C_{2n}. The capacitors C_3-C_{2n+1} also release energy to the load. The current-flow path is shown in Fig. 3(h). This mode ends at t = t_6 when the current ip reaches to zero at the beginning of the next switching period.

III. Steady-State Analysis of the Proposed Converter

A. *Steady-State and Voltage-doubling Circuit Analysis of the Equivalent Circuit*

This section adopted Fundamental-Sinusoidal analysis to analyze the converter carried out under the basic assumptions in the second section. First, the resonant inductor current is sinusoidal, and the harmonic components are neglected. In addition, in order to analyze the output voltage ripple, the proposed voltage-doubling circuit could be equivalent as the one shown in Fig. 4. The voltage-doubling circuit of the capacitors C_1-C_{2n+1} and C_2-C_{2n} is equivalent to the capacitor C_{eq} and the high voltage load R_L is equivalent to the load R_{eq}. Finally, if the capacitor C_{eq} and the load R_{eq}

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are transformed to C_o and R_o on primary side of the high voltage high frequency transformer, the quality factor Q, leakage inductor L_r, and resonant capacitor C_r can be designed more conveniently.

The output voltage v_{ab} of inverter bridge is an AC square wave having the same frequency as switching frequency. In order to simplify the following analysis, the Fourier analysis is adopted. Thus, the waveform v_{ab} is approximately a sinusoidal wave v_{ab1}. As shown in Fig. 5, v_{ab1} could be written as:

$$v_{ab1}(t) = \frac{4}{\pi} \cdot \mathrm{V}_{in} \sin(\omega_s t) \quad , \tag{1}$$

where ω_s is the switching angular frequency and can be expressed as

$$\omega_s = 2\pi f_s \, . \tag{2}$$

Because the resonant inductor current is assumed to be sinusoidal, i_{Lr} can be derived according to Fig. 5.

$$i_{Lr}(t) = I_{Lr,pk} \sin(\omega_s t - \gamma) \quad , \tag{3}$$

where γ is the lagging phase angle with v_{ab1}.

According to the circuit topology in Fig. 1, input source is connected with resonant inductor L_r, so input current I_{in} can be expressed as:

$$I_{in} = \frac{1}{\pi} \int_0^{\pi} i_{Lr}(t) d\omega_s t = \frac{2I_{Lr,pk} \cos(\gamma)}{\pi} \quad 。 \tag{4}$$

η is the conversion efficiency and can be written as

$$v_{ab1,rms} i_{ab,rms} \eta = V_o I_o \quad , \tag{5}$$

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Substituting the equation (4) into the equation (5), then the maximum value of resonant inductor current $I_{Lr,pk}$ is obtained as:

$$I_{Lr,pk}(\gamma) = \frac{\pi V_o I_o}{2\eta V_{in} \cos(\gamma)} \quad 。 \tag{6}$$

During the conduction interval of energy transfer from primary side to the load, the equation of current i_p could be expressed as:

$$i_p(t) = \begin{cases} -I_{p,pk} \sin(\frac{\pi}{2\alpha}\omega_s t) & 0 \le \omega_s t \le \alpha \\ -I_{p,pk} \sin(\frac{\pi}{2(\theta-\alpha)}(\omega_s t - \theta - \alpha)) & \alpha \le \omega_s t \le \theta \end{cases} \quad , \tag{7}$$

Because the mean current i_p in half period is equal to the output current, the $I_{p,pk}$ could be derived as:

$$\mathrm{I}_{p,pk}(\theta) = \frac{I_o NK\pi^2}{2\theta\eta} \quad 。 \tag{8}$$

where θ affects the energy transfer of the current i_p from primary to secondary side of the transformer. In addition, when a higher value is chosen for the phase angle θ, the output voltage ripple will be smaller. The above problem will be discussed below. Thus, the phase angle θ is a very important parameter.

Parameters in Fig. 5, including α, β, γ, and δ, are based on v_{ab1}. α is the phase angle that represents i_p going from zero to negative peak value when v_{ab1} is positive. β is the phase angle that the current i_{Cr} lags behind v_{ab1}. γ is the phase angle that the current i_{Lr} lags behind v_{ab1}. Thus, δ can be expressed as:

$$\delta = \theta - \gamma \quad 。 \tag{9}$$

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The parameters θ, α, β, γ, and δ related to component design and output voltage ripple are very important. Because the mean value of current i_p in half period is equal to the output current, the phase angle θ is in relation to the output power value. Then, the negative maximum value of current $I_{p,pk}$ could be decided by the phase angle α. Actually, the output voltage ripple was decided by phase angle θ and phase angle α. The output voltage ripple is discussed below. Furthermore, the phase angle γ can be decided and is related to whether the power switch S_a-S_d can achieve ZVS turn on or not. If the phase angle β were much smaller, the current $I_{p,pk}$ would increase certainly. As the value of the current $I_{p,pk}$ lowers, the size of the phase angle β increases.

According to Kirchhoff's Current Law, the resonant capacitor current i_{Cr} can be formulated as the following equations:

$$i_{Cr}(t)=\begin{cases} i_{Lr}(t)-i_p(t) & 0\le\omega_s t\le\theta \\ i_{Lr}(t) & \theta\le\omega_s t\le\pi \end{cases}, \tag{10}$$

During the interval of the resonant capacitor current i_{Cr}, the peak value and phase could be found based on Fourier transform.

$$i_{Cr}(\alpha,\gamma,\theta)=C(\alpha,\gamma,\theta)\angle\sigma(\alpha,\gamma,\theta), \tag{11}$$

where $C(\alpha,\gamma,\theta)$ is the resonant capacitor current i_{Cr} waveform coefficient

$$C(\alpha,\gamma,\theta)=\sqrt{a^2(\alpha,\gamma,\theta)+b^2(\alpha,\gamma,\theta)}, \tag{12}$$

where $a(\alpha,\gamma,\theta)$ and $b(\alpha,\gamma,\theta)$ are below in the equations (13) and (14).

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$$\mathrm{a}(\alpha,\gamma,\theta)=-I_{Lr}\sin(\gamma)+\frac{I_p}{\pi}\cdot\left\{\frac{1}{\frac{\pi}{2\alpha}+1}[\sin(\alpha)+1]-\frac{1}{\frac{\pi}{2\alpha}-1}[\sin(\alpha)-1]\right\}$$
$$+\frac{I_p}{\pi}\cdot\left\{\frac{1}{\frac{\pi}{2(\theta-\alpha)}+1}[\cos(\theta)-\sin(\alpha)]-\frac{1}{\frac{\pi}{2(\theta-\alpha)}-1}[\cos(\theta)+\sin(\alpha)]\right\}, \quad (13)$$

$$\mathrm{b}(\alpha,\gamma,\theta)=I_{Lr}\cos(\gamma)+\frac{I_p}{\pi}\cdot\cos(\alpha)\left(\frac{1}{\frac{\pi}{2\alpha}-1}-\frac{1}{\frac{\pi}{2\alpha}+1}\right)$$
$$+\frac{I_p}{\pi}\cdot\left\{\frac{1}{\frac{\pi}{2(\theta-\alpha)}-1}[\sin(\theta)-\cos(\alpha)]-\frac{1}{\frac{\pi}{2(\theta-\alpha)}+1}[\sin(\theta)+\cos(\alpha)]\right\}, \quad (14)$$

The phase angle of the resonant current i_{Cr} can be expressed as equation (15) by Fourier transform.

$$\sigma(\alpha,\gamma,\theta)=\tan^{-1}\left(\frac{a(\alpha,\gamma,\theta)}{b(\alpha,\gamma,\theta)}\right), \quad (15)$$

The phase angle $\sigma(\alpha,\gamma,\theta)<0$ because $a(\alpha,\gamma,\theta)<0$ and the equation (15) also can be expressed as:

$$\sigma(\alpha,\gamma,\theta)=\angle\beta \quad (16)$$

The phase angle β should be as large as possible because the current $I_{p,pk}$ can decrease certainly. In equation (8), if the current $I_{p,pk}$ were decreased, the phase angle θ became large certainly. In Fig. 2, the output voltage ripple is in relation to the current $I_{p,pk}$. In order to simplify the output voltage ripple analysis, the following conditions are assumed when the negative maximum value of current i_p approaches the half angle of θ. Therefore, the phase angles $\alpha \approx \theta/2$. Then, the output voltage ripple was developed by the equivalent capacitance C_{eq}. According to the law of conservation of energy, the energy of leakage inductor L_p is totally transferred to the equivalent capacitance C_{eq}, and the equation can be written as:

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$$L_p \cdot I_{p,\max}^2 = \frac{1}{2} \cdot C_{eq} \cdot \left(V_{o,\max}^2 - V_{o,\min}^2 \right) \quad (17)$$

Furthermore, the current i_p is approximately sinusoidal waveform, so the negative peak value of the current i_p is not the maximum value. In half period, the actual waveform i_p and approximate waveform i_{p1} should transfer the same energy from primary side to secondary side of the high frequency high voltage transformer T_r, so the mean value of current i_p is equal to that of the current i_{p1}. The maximum value of current i_{p1} could be derived as:

$$\mathrm{I}_{p,pk}^2 = I_{p,\max}^2 \cdot \frac{\pi}{\theta} \quad (18)$$

The output voltage of the proposed converter can be expressed based on Fig. 1.

$$\mathrm{V}_o = (4n+1) \cdot \mathrm{V}_m \quad (19)$$

where n is the stage number of voltage-doubling circuit and V_m is the high side voltage of the transformer.

Hence, the parameter K can be defined as:

$$\mathrm{K} = 4n+1 \quad (20)$$

In addition, the voltage gain from the voltage v_{ab1} to the resonant capacitor voltage can be derived as:

$$\mathrm{M}_{\mathrm{vr}} = \frac{\mathrm{V}_{Cr}}{V_{ab,rms}} \quad (21)$$

Then, the turn ratio N of the transformer could be developed by the equation (20) and (21). The turn ratio can be expressed as:

$$\mathrm{N} = \frac{V_o}{K\mathrm{V}_{in} \cdot M_{vr}} \quad (22)$$

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In Fig. 2, during the Mode II, the output voltage goes from minimum to maximum, so the output voltage ripple could be decided. Then, the output voltage ripple can be expressed as:

$$V_{o,ripple} = \frac{V_{o,\max} - V_{o,\min}}{V_o} \quad (23)$$

Substituting equation (18) and (23) into the equation (17), then the output ripple $V_{o,ripple}$ can be expressed as the following:

$$V_{o,ripple} = \frac{L_p \cdot I_{p,pk}^2}{C_{eq} \cdot V_o^2} \cdot \left(\frac{\theta}{\pi}\right) \quad (24)$$

where C_{eq} is the equivalent capacitance of the voltage-doubling circuit in Fig. 4. In equation (24), the output voltage ripple is related to the parameter between the phase angle θ and the current of the negative value $I_{p,pk}$. Due to the current value $I_{p,pk}$ is decided by the phase angle α, the output voltage ripple is in relation to the phase angle α and θ by equation (24).

Substituting the equation (8) into the equation (24), then the output ripple could be rewritten as follows:

$$V_{o,ripple} = \frac{L_p N^2 K^2 \pi^3}{4\eta^2 R_L C_{eq} \theta} \quad (25)$$

IV. Design Parameter of the Proposed Converter

In order to simplify the component design, the leakage inductor L_p and equivalent capacitance C_o are neglected. Hence, R_o can be calculated by equation (5) and it could be derived as:

$$R_o = \frac{R_L \cdot \eta \cdot \cos(\gamma)}{2N^2 K^2} \quad (26)$$

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In Fig. 6, the voltage gain of resonant tank can be expressed as:

$$M_{vr} = \frac{4}{\pi} \cdot \frac{1}{\sqrt{\left(1-\frac{f_s}{f_r}\right)^2 + \left(\frac{1}{Q}\left(\frac{f_s}{f_r}\right)\right)^2}} \quad (27)$$

where f_r is the resonant frequency, Q is the quality factor and can be defined as:

$$\mathrm{Q} = \omega_r \cdot C_r \cdot R_o = \frac{R_o}{\omega_r \cdot L_r} \quad (28)$$

Substituting the equation (25) and (26) into the equation (28), then the relation between quality factor Q and phase angle θ can be derived as:

$$\mathrm{Q} = \frac{L_p \cdot \pi^3 \cdot Cos(\gamma)}{8\eta \cdot C_{eq} \cdot \theta \cdot \omega_r \cdot L_r} \quad (29)$$

If a higher value was chosen for the phase angle θ, the quality factor would be low. In order to reduce the output voltage ripple, a higher value was chosen for the phase angle θ, but the voltage gain M_{vr} was limited based on Fig. 6. Hence, it can trade off between output voltage ripple and voltage gain M_{vr}. In addition, the output voltage ripple was reduced base on equation (24), because a lower value is chosen for the peak value $I_{p,pk}$. Simultaneously, according to the Fig. 7, lower peak value Ip,pk could make whole efficiency rising up.

Fig. 8 shows the correlations between the current $I_{Lr,pk}$ and the phase angle γ at efficiency of 0.7, 0.75 and 0.8 respectively, so it would be better to choose a higher phase angle γ. The quality factor Q and voltage gain of M_{vr} could be decided by Fig. 6. Hence, the frequency ratio was also decided. Substituting the equation (26) into the equation (28), the resonant inductor L_r and C_r can be calculated.

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According to the law of conservation of energy, the resonant inductor L_r transfers energy to the parasitic capacitance of the power switch. In order to make power switches S_a-S_d achieve ZVS, the equation (30) must be satisfied, and can be expressed as:

$$L_r \cdot I_{Lr,pk}^2 \geq 2C_{oss} \cdot V_{ds}^2 \quad 。 \tag{30}$$

V. EXPERIMENTAL RESULTS OF THE PROPOSED CONVERTER

TABLE I

SYSTEM SPECIFICATION

Specification	Value
Input voltage V_{in}	400 Vdc
Output voltage V_o	40 kVdc
Output voltage ripple $V_{o,ripple}$	<5%
Load resistance R_L	5.33 MΩ
Switching frequency ω_s	80 kHz
Resonant frequency	50 kHz
Output power P_o	300 W
MOSFET S_a-S_d	IXFH36N60P
High voltage Diode D_1-D_9	2CL2FM

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TABLE II

SYSTEM PARAMETERS

Parameter	Value
Leakage inductor L_p	63.56 μH
Resonant inductance L_r	1.61 mH
Resonant capacitance C_r	27.2 nF
Capacitors $C_{1\text{-}9}$	3.0 nF
Quality factor Q	3
Voltage gain M_{vr}	1.8
Turn ratio N (N_s / N_p)	4.8

TABLE III

EXPERIMENT RESULTS

	M_{vr}	N	K	θ	γ	$I_{Lr,pk}$	$I_{p.pk}$
Experiment values	1.84	4.82	9.02	72.0	64.8	3.43	1.87
Parameter values	1.8	4.8	9	70	60	3.36	1.86

To demonstrate the performance of the proposed converter, a prototype circuit is implemented in the laboratory. The specifications and parameters of the DC-DC resonant converter are shown in table I and table II. Then, the experiment results and parameter values are shown in table III. In Fig. 9, waveforms of v_{AB} and i_{Lr} show that the voltage leads the current which allows all switches to achieve ZVS turn on. In addtion, both the current of resonant inductor and leakage inductor value

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are approaches the designing value. Thus, the proposed analytical methodology is feasible. Finally, the waveforms are verified and the performance of the proposed converter is at full load when the input voltage V_{in}=400V, the output voltage V_o=40kV, and the output power P_o=300W. In Fig. 10, the waveforms show the voltage across the transformer's primary side v_p and the voltage across the leading leg switches' and the lagging leg switches' neutral point v_{AB}. The transfer gain ratio M_{vr} between v_{Cr} and v_{AB} can be easily calculated. Therefore, the experiment is shown in Table III. In Fig. 11(a) and 11(b), gate signals of the switches S_a-S_d and the voltage stress across these switches are shown, respectively. It can be seen that all the switches achieve ZVS turn on. In Fig. 12, the waveforms show the voltage across the transformer's primary side v_{Cr} and the voltage across the transformer's secondary side v_s. The turn ratio N of the high-frequency high-voltage transformer can be calculated easily. Hence, the experimental result approaches the parameter values. In Fig. 13, the waveforms show the output voltage ripple $V_{o,ripple}$ and the current i_p. It could be easily observed that the output voltage ripple is correlated to the current i_p. Furthermore, no matter the phase angle and output voltage ripple are in the anticipate range. In this paper, the topology has a very low output voltage ripple 4.1%. Comparing it with the topology in literature [11], the difference between the two topology is about 2%. Consequently, the experiment result is near to the parameter values. Table III compares between difference of the parameter values and experiment values. It is obvious that the difference is very low. In Fig. 14, using the soft start to aviod the output voltage occurring the overshoot and making the output being regulated at 40kV. Finally, the whole

efficiency of the proposed converter circuit is showed in the Fig. 15, and the highest efficiency is 78.8% at full load.

VI. CONCLUSIONS

A novel voltage-doubling circuit with parallel resonant DC-DC converter is proposed in this paper. It can not only reach a higher output voltage but also reduce the output voltage ripple. In this paper, the output voltage ripple is 4.1%, and it's much lower than the conventional one. Using basic sinusoidal waveform analytical method, it can decide not only the output ripple but also the capacitance of the voltage-doubling circuit. This paper adopted the phase-shift control technique to adjust output power. Then, using this technique with the parallel resonant tank makes all the power switches S_a-S_d achieve zero voltage switching (ZVS). This technique can be applied to different power conversion systems easily. The design values and experimental results are shown. The whole efficiency of the proposed converter circuit is showed in the Fig. 15, and the highest efficiency is 78.8% at full load. A prototype circuit with input voltage 400V, output voltage 40kV, and output power 300W is developed in the laboratory.

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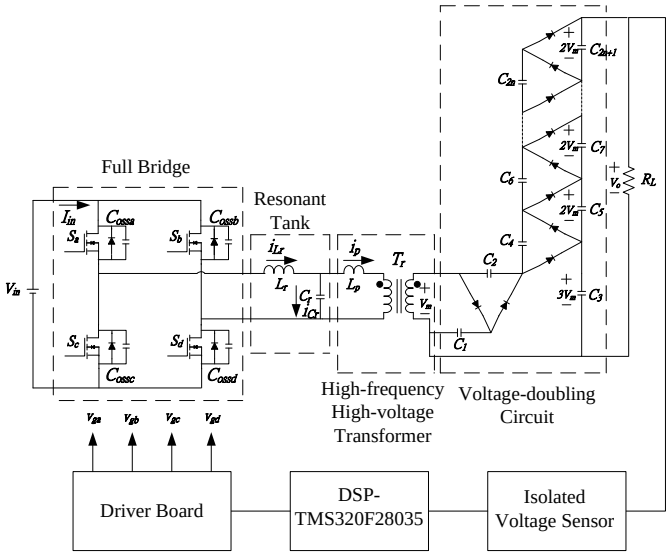

Fig. 1. Schematic of a novel DC-DC converter circuit and system

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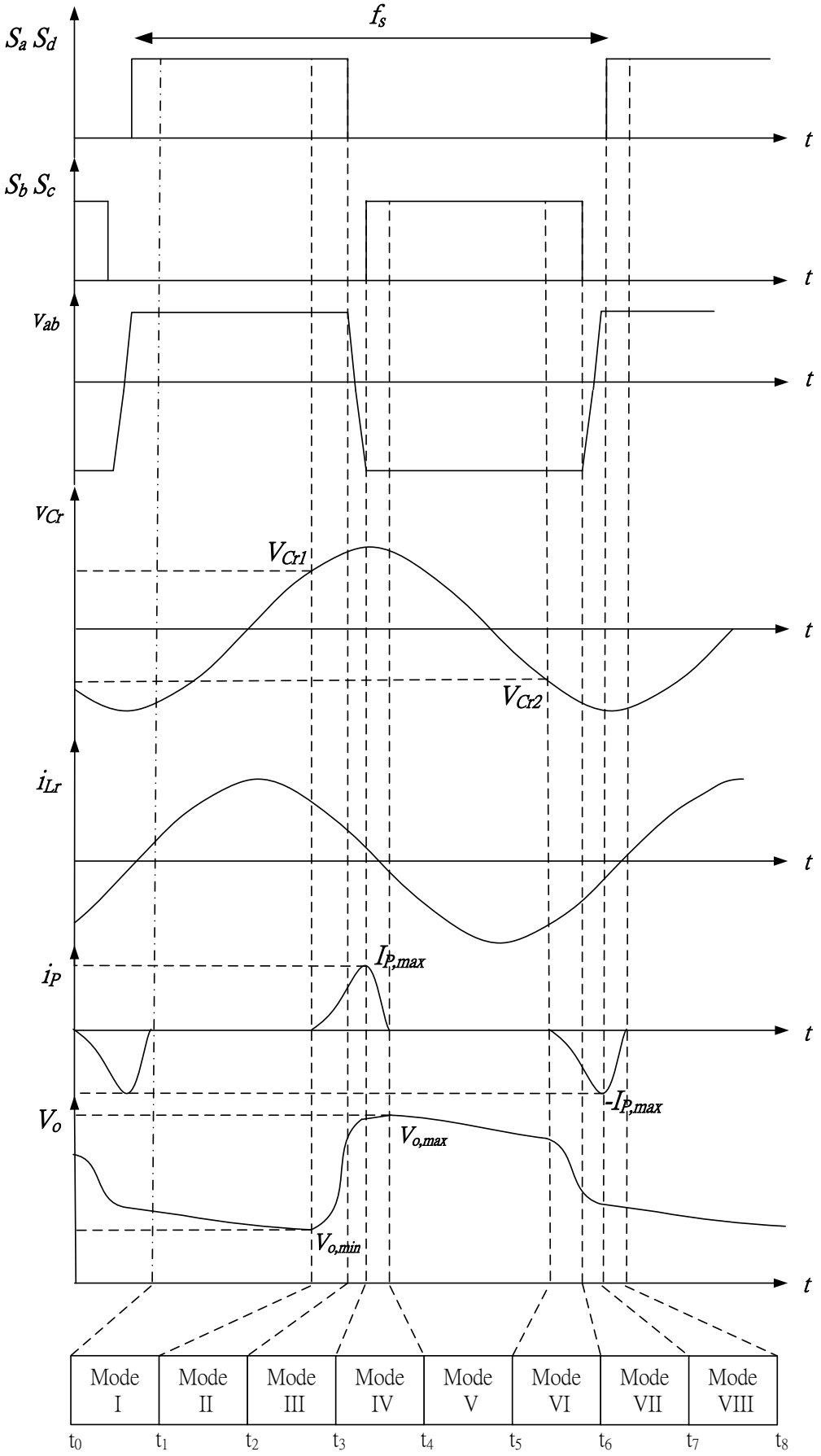

Fig. 2. Key waveforms of a novel DC-DC converter circuit

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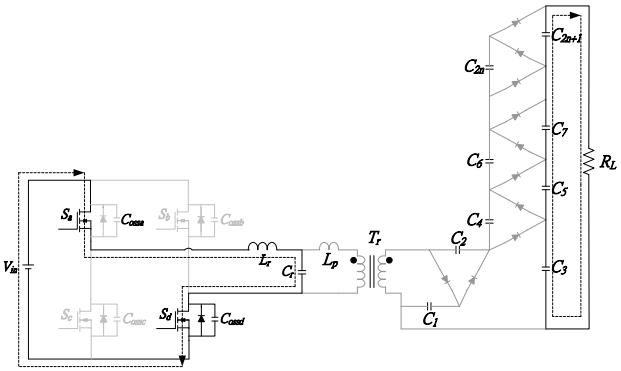
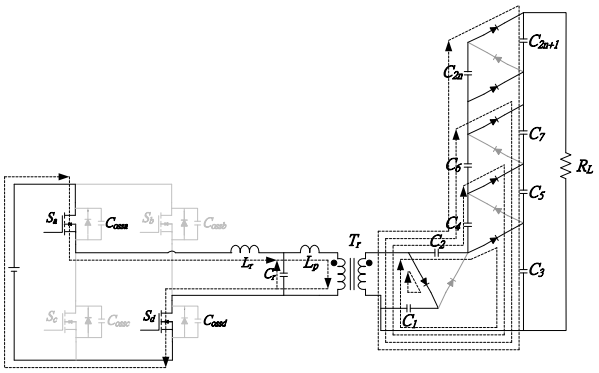
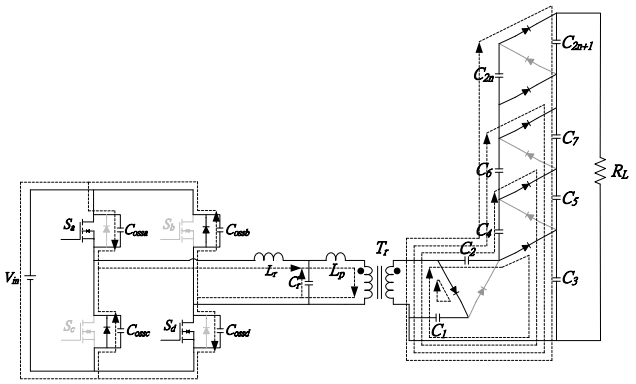


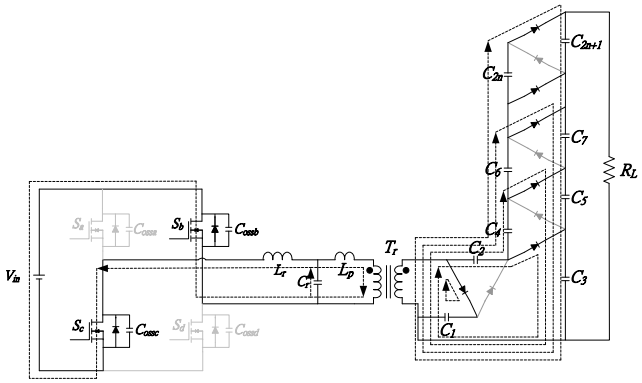
(a) Mode I [t_0-t_1]



(b) Mode II [t_1-t_2]



(c) Mode III [t_2-t_3]



(d) Mode IV [t_3-t_4]

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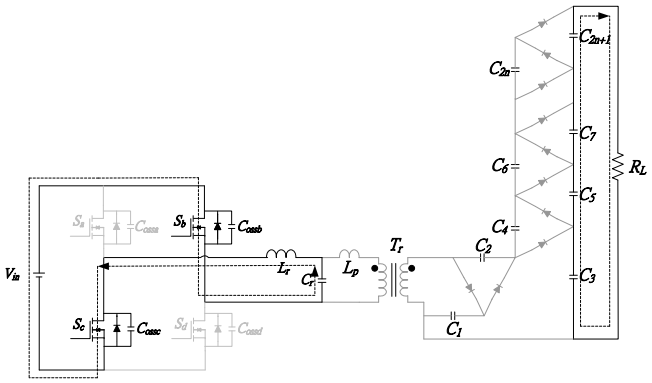
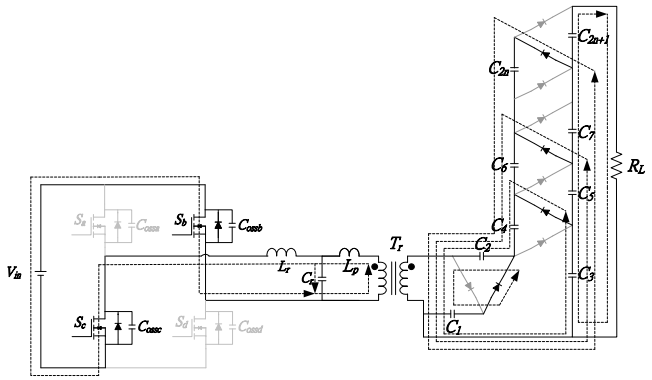
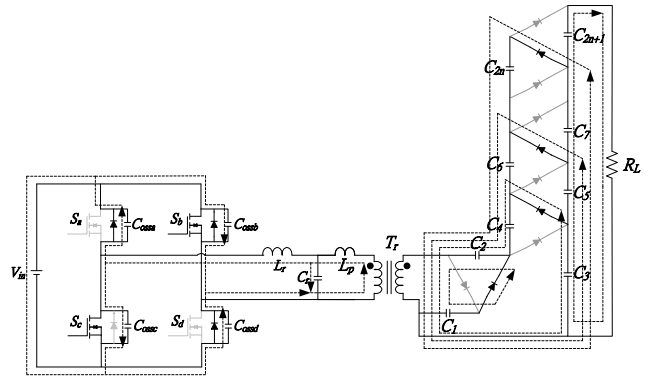


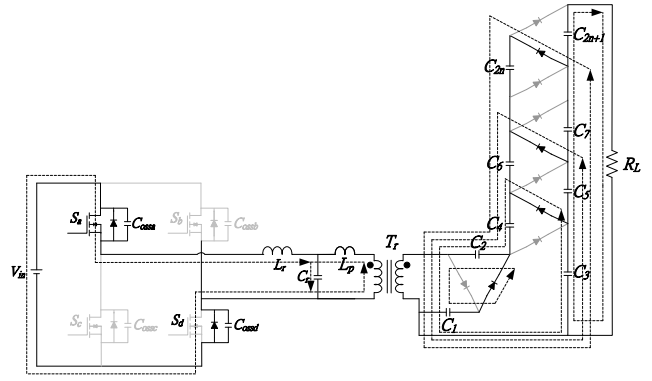
(e) Mode V [t_4-t_5]



(f) Mode VI [t_5-t_6]



(g) Mode VII [t_6-t_7]



(h) Mode VIII [t_7-t_8]

Fig. 3. Current-flow paths of the operating modes during one switching period (a) Modes I. (b) Modes II. (c) Mode III. (d) Mode IV. (e) Modes V. (f) Modes VI. (g) Modes VII. (h) Modes VIII.

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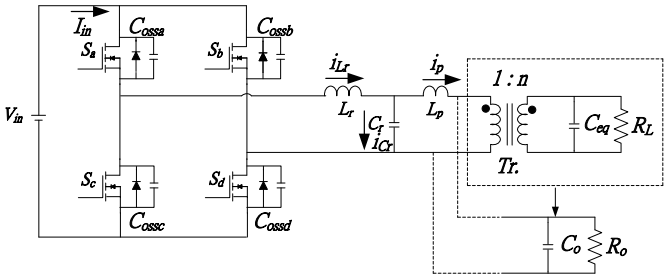

Fig. 4. The equivalent circuit of the proposed converter

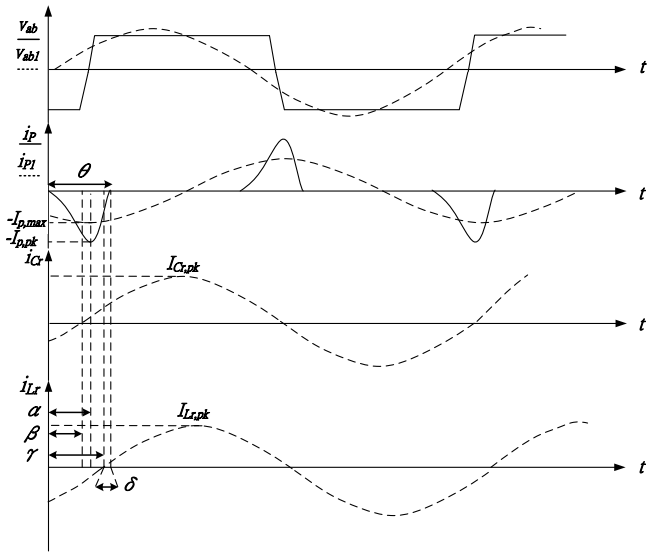

Fig. 5. Analysis of the proposed converter under steady state

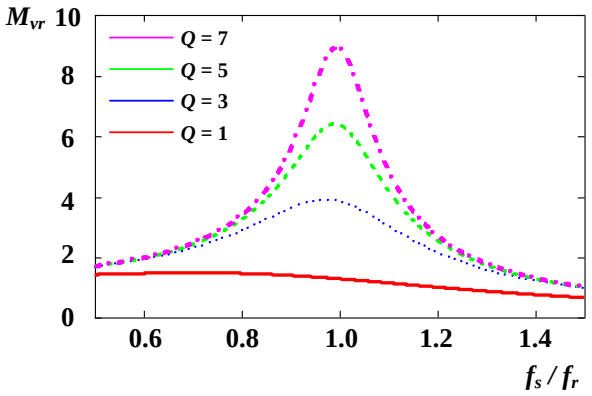

Fig. 6. The voltage gain of the parallel resonant tank

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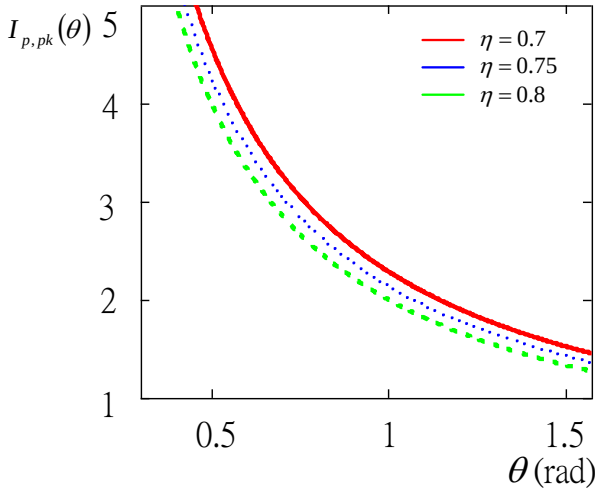

Fig. 7. The relation between the peak current $I_{p,pk}$ and the phase angle θ

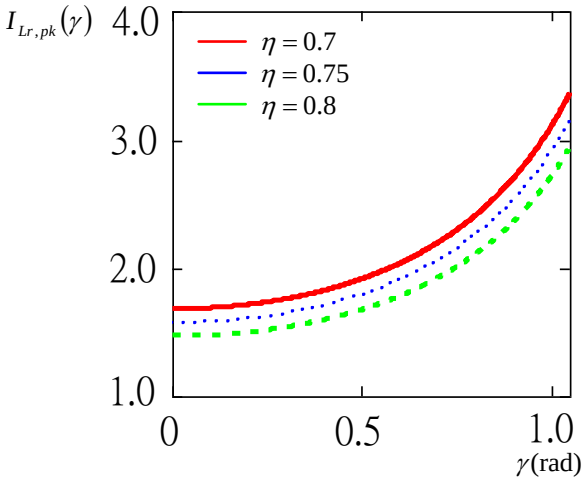

Fig. 8. The correlation between the peak current $I_{Lr,pk}$ and the phase angle γ

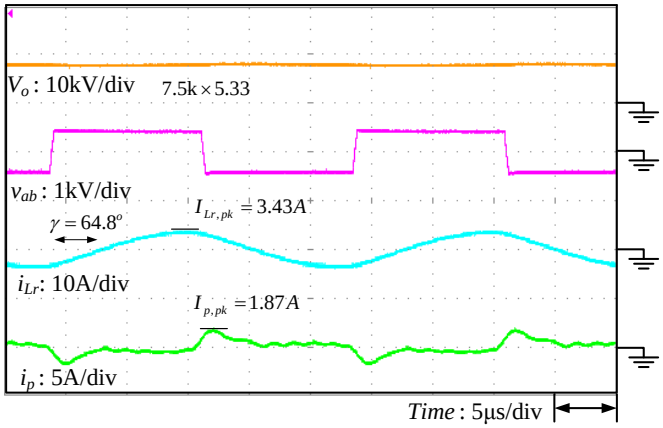

Fig. 9. Experimental results at full load P_o=300W.

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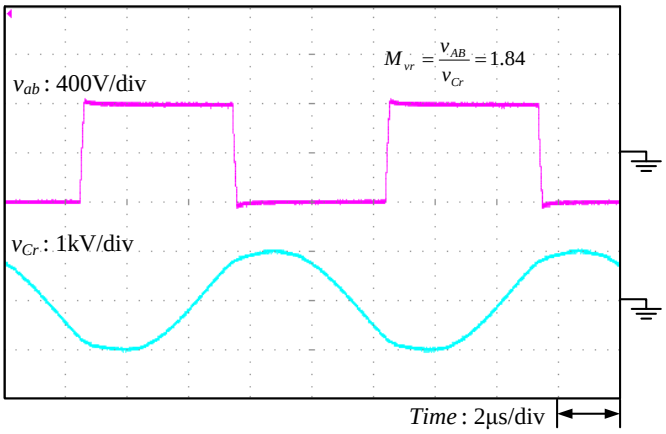
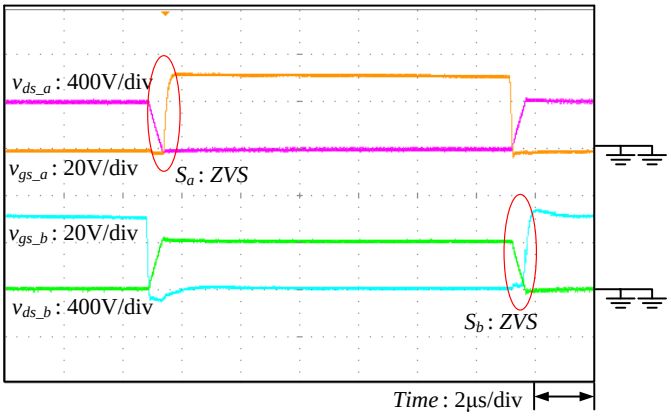
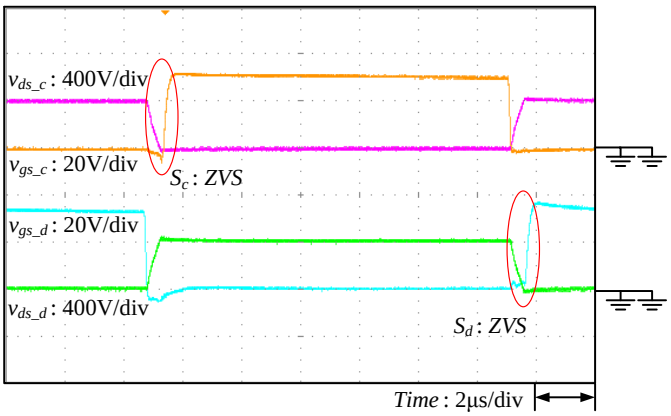


Fig. 10. Experimental results of voltage v_{Cr} and v_{ab}.



(a)



(b)

Fig. 11. The signal and voltage stress in switches S_a - S_d at full load P_o = 300W.

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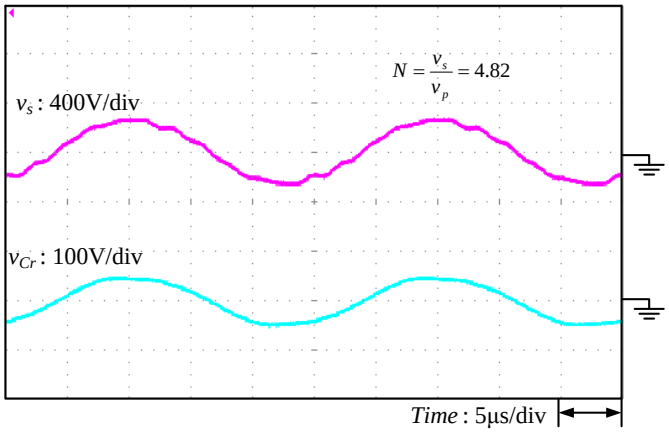

Fig. 12. Experimental results of voltage v_p and v_s.

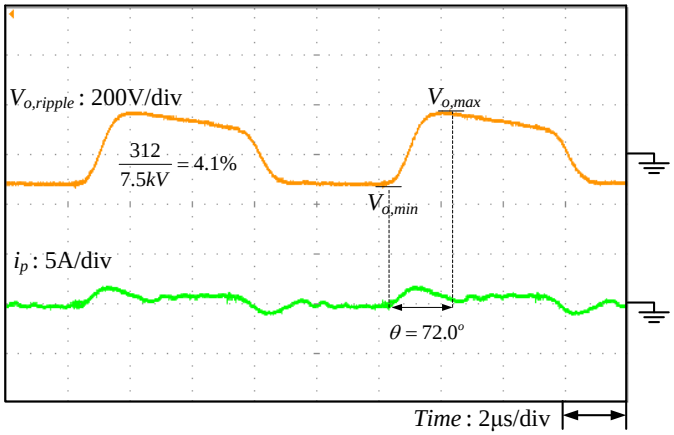

Fig. 13. Experimental results of output voltage ripple $V_{o,ripple}$ and leakage inductor current i_p.

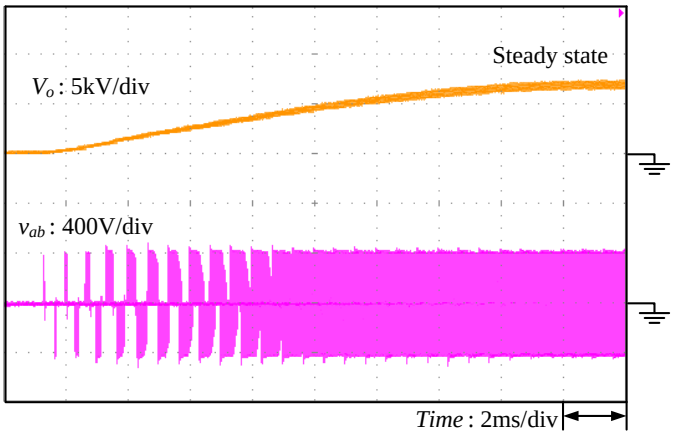

Fig. 14. Experimental results of output voltage at starting up and steady state.

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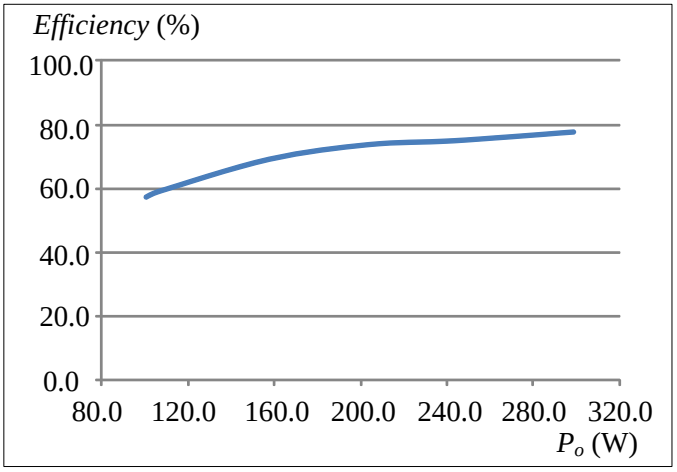

Fig. 15. Experimental results of the whole efficiency in the proposed converter.