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A Low-power Incremental Delta-Sigma ADC for CMOS Image Sensors

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***Abstract*— This paper presents a 2nd-order incremental delta-sigma ADC for CMOS image sensors. The ADC employing a cascade of integrators with feedforward (CIFF) architecture uses only one operational transconductance amplifier (OTA) by sharing the OTA between 1st and 2nd stages of the modulator. Further power and area savings are achieved by using a self-biasing amplifier and the proposed level-shifting technology which allows active signal summation at the quantizer input node without using an additional OTA. Fabricated in 0.18-µm CMOS image sensor process, the 10-bit ADC occupies a die area of 0.002mm^2 and consumes 29.5 µW from a 1.8V supply. The measured DNL and INL are less than +0.22/-0.2 LSB and +0.71/-0.89 LSB, respectively. Operating at 20MS/s, the ADC provides SNDR of 57.7dB and 62.3dB for a signal bandwidth of 156.25kHz and 78.125kHz, respectively.**

***Index Terms*—Analog to digital converter (ADC), delta-sigma (ΔΣ) modulator, cascade of integrators with feedforward (CIFF), amplifier sharing, self-bias amplifier, CMOS image-sensor (CIS).**

I. Introduction

Ever-increasing demand for high-resolution, high-frame rate, and low-power CMOS image sensors makes the design of pixel readout circuits, especially analog-to-digital converters (ADCs), a challenging task. Although single-slope ADCs [1] have been widely used in the column-parallel ADC architecture due to their simplicity, the ADC conversion time exponentially grows as the ADC resolution increases. For example, an N-bit conversion requires 2^N clock cycles, limiting the frame rate of CMOS image sensors. Recently, delta-sigma ADCs have successfully demonstrated their usefulness for array implementations with superior noise performance and faster conversion speed than those of single-slope ADCs. However, operational transconductance amplifiers (OTAs) used in delta-sigma modulators often take up a considerable amount of power and die area. In addition, biasing more than thousands of OTAs is not a trivial task [2]. Sharing a bias voltage through a long metal line between the OTAs makes the bias voltage susceptible to noise coupling or incomplete settling after switching events. Current-mode biasing schemes require thousands of metal lines to carry bias currents to OTAs and can waste a significant amount of die area and power.

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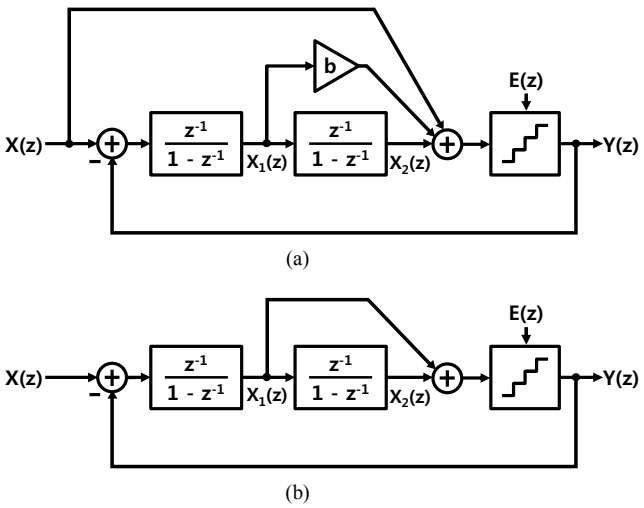

Fig. 1. CIFF modulator architectures. (a) with input feedforward path. (b) without input feedforward path.

In this work, a self-biased amplifier proposed in [3] has been adapted to relax the biasing issue. In order to further save power, the amplifier has been modified to be shared by adjacent integrators without being affected by residual charge stored on the amplifier's input parasitics. A second-order delta-sigma ADC employing the amplifier has been proposed and implemented in a 0.18-μm CMOS image sensor process. While taking up only a die space of 0.002mm^2, the ADC achieves 10-bit accuracy and draws the total current of 16.4μA from a 1.8V supply, resulting in a FOM of 151fJ/Conv.-step.

This paper is organized as follows. Section II introduces the delta-sigma modulator and its operational principle. Implementation details of the amplifier and modulator are explained in section III. Measurement results and conclusions are provided in section IV and V, respectively.

II. Proposed Delta-Sigma Modulator

Two popular second-order modulator architectures, known as a cascade of integrators with feedforward (CIFF) with and without input feedforward path, are shown in Fig. 1. It is

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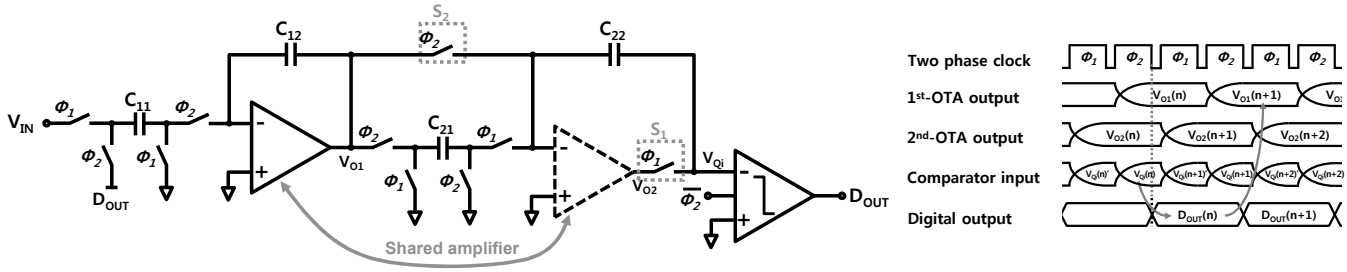

Fig. 2. Schematic diagram of CIFF modulator without input feedforward path and timing diagram.

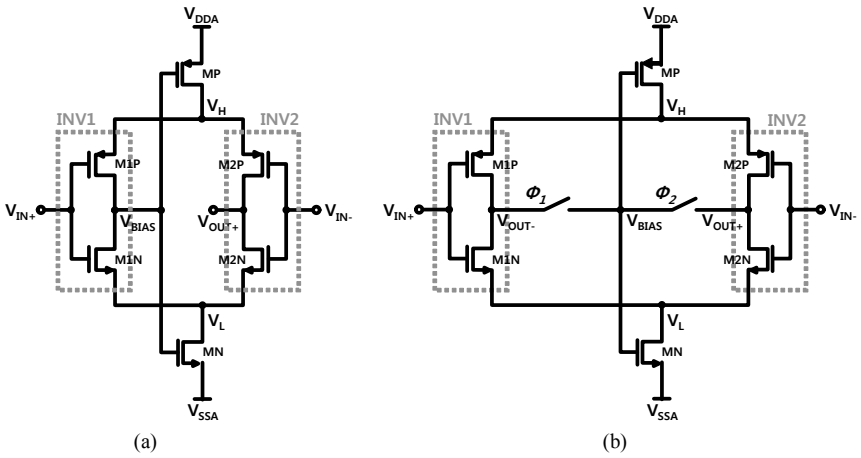

Fig. 3. Self-bias amplifier. (a) Amplifier in [3]. (b) Proposed amplifier.

well-known that the signal feedforward path relaxes gain and bandwidth requirements of the OTAs by removing the input signal component from the loop filter. However, analog signal summation at the quantizer input, which can be performed either passively or actively, requires additional power and die space [4]. While the direct input signal feedforward path in Fig. 1(a) allows elimination of the input signal component in the loop filter, the first stage (OTA) in Fig. 1(b) has the high-pass filtered input signal at its output.

The CIFF architecture without input feedforward path has been chosen in this work because of two reasons. First, the pixel output behaves like a DC signal, thus the first integrator has a negligible output swing even without the direct input signal feedforward path. Second, the proposed level-shifting technique which will be explained shortly allows active signal summation without increasing power consumption or hardware complexity.

A simplified schematic of the proposed modulator and associated timing diagram are shown in Fig. 2. Notice that hardware complexity is almost the same as the simple second-order modulator without the input signal feedforward path [5] except for two additional switches, S_1 and S_2. S_1 is added to share the OTA between the integrators, which will be explained in the next subsection, and S_2 directly connects the first integrator output to the feedback capacitor of the second integrator (C_{22}). The modulator operates with two-phase non-overlapping clocks. The input signal is sampled by a sampling capacitor of the first integrator (C_{11}) during phase Φ_1. At the same time, the second integrator performs signal integration and the voltage across C_{22} becomes $V_{o2}(n)$. In the next phase Φ_2, the charge on C_{11} is transferred to the feedback capacitor C_{12} and the first integrator output is connected to the bottom plate of C_{22} through S_2. Since the top plate of C_{22} is floating by turning off S_1, its node voltage becomes $V_{o1}(n) + V_{o2}(n)$. Shifting the voltage across C_{22} ($V_{o2}(n)$) by $V_{o1}(n)$, which is called a level-shifting technique, performs active summation of the first and second integrator outputs. Then the comparator makes a decision with the summed voltage at the falling edge of Φ_2 and the rest of the modulator operates like a conventional modulator.

III. Amplifier Sharing using Self-biased Amplifier

As briefly explained in the introduction, biasing the amplifiers in the array application is not a trivial task.

In [6], an inverter was used as an amplifier and successfully applied to a second-order delta-sigma modulator. However, the inverter causes two potential problems. First, current flowing through the inverter cannot be well defined. In [6], the transistor size was chosen carefully to minimize short-circuit current, however, the current can vary significantly due to process, voltage, and temperature (PVT) variations. Hence, a regulator has been introduced in [7], which also requires die area and power consumption. Second, an additional capacitor and switches are required to define the input common-mode voltage of the inverter to be used in a switched-capacitor integrator. This does not only take up die space, but also increases kT/C noise when the common-mode voltage is sampled on the capacitor.

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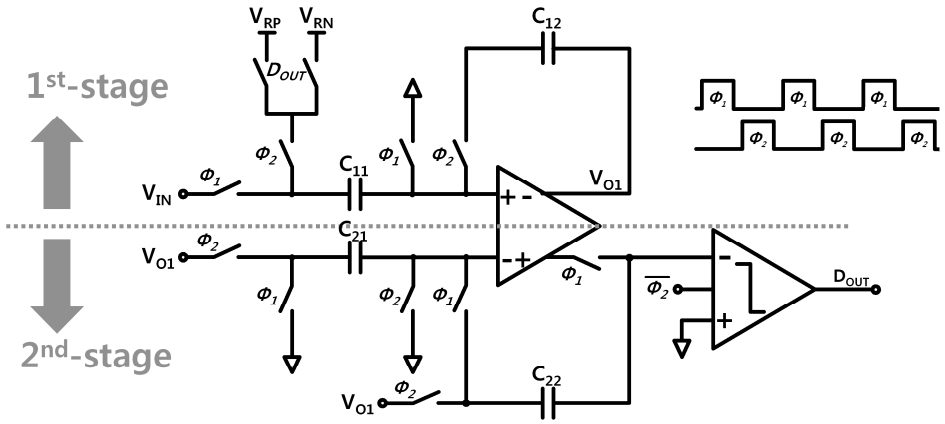

Fig. 4. Circuit implementation of proposed delta-sigma modulator.

TABLE I
SIZE AND OPERATION REGION

		W(μm)	L(μm)	I(μA)	Operation region
MP		1.39	0.325	10.16	Triode
MN		0.71	0.8	10.16	Triode
INV1	M1P	3.4	2.4	5.08	Saturation
	M1N	0.6	2.56	5.08	Saturation
INV2	M2P	3.4	2.4	5.08	Saturation
	M2N	0.6	2.56	5.08	Saturation

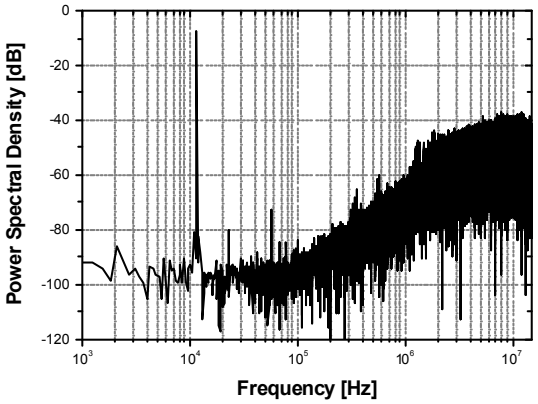

Fig. 6. Measured dynamic performance.

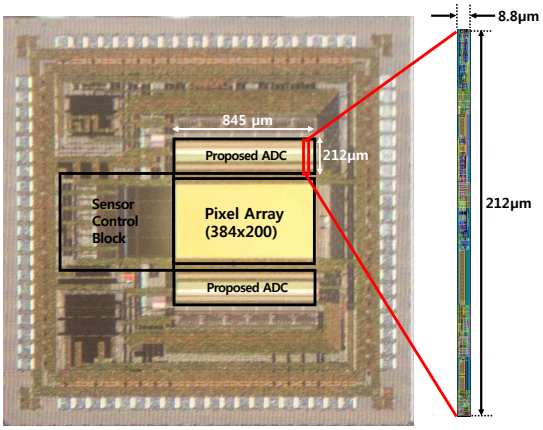

Fig. 5. Die micrograph.

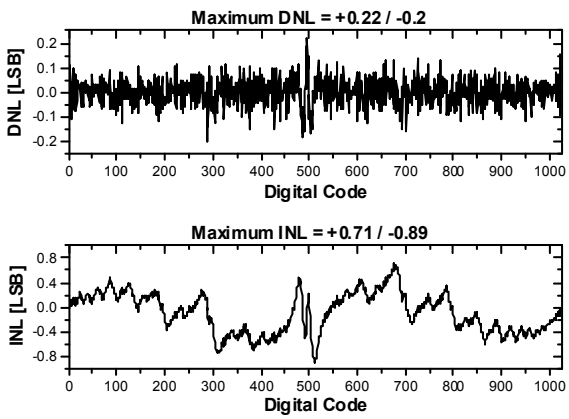

Fig. 7. Measured static performances.

Aforementioned issues can be relaxed by using a self-biasing scheme. As shown in Fig. 3(a), the amplifier has two inverters connected in parallel whose current is regulated by an upper PMOS (MP) and lower NMOS (MN) transistor through negative feedback. While one inverter (INV2) amplifies an input signal, the other one (INV1) establishes the amplifier's bias condition. In this work, as in Fig. 3(b), two switches, driven by two-phase non-overlapping clocks, are added to allow the inverters to exchange roles. While INV1 works as an amplifier for the first integrator, INV2 sets the bias current (Φ_2). In the next phase (Φ_1), INV2 integrates the charge from the first integrator and INV1 sets the bias current. Schematic of the modulator is shown in Fig. 4. It is implemented in a single-ended configuration as pixels generate a single-ended

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TABLE II

PERFORMANCE COMPARISON

Reference	[9]	[10]	[11]	[12]	[13]	[14]	[15]	**This design**
Technology	65-*nm*	0.13-μm	0.13-μm	0.13-μm	0.18-μm	0.13-μm	0.35-μm	**0.18-μm**
Sampling rate [MS/s]	150	1.6	48	1.4	3.2	80	2.4	**20**
Signal bandwidth [kHz]	200	8	218	10	100	5000	20	**156.25**
Supply voltage [V]	-	1.2	1.2	0.25	1.5	1.2	1.5	**1.8**
SNDR [dB]	77	56	66	61	84	70.7	87.9	**57.7**
Power consumption [mW]	0.95	0.0048	0.04	0.0075	0.14	8.1	0.14	**0.0295**
Active area [mm^2]	0.03	0.03	0.0027[1)]	0.3375	0.49	0.37	0.207	**0.0018656**
FOM [fJ/Conv.step]	410	582	56	409	54	289	172	**151**
FOM_A [fJ·mm^2/Conv.step]	12.3	17.5	0.152	138	26.5	107	35.7	**0.281**
Architecture	Inverter-based	Self-biased Super Inv.	Inverter-based	Inverter-based	3rd-order single amp	8b 2-step quantizer	Inverter-based	**Self-biased amplifier**

1) including decimation filter and memory

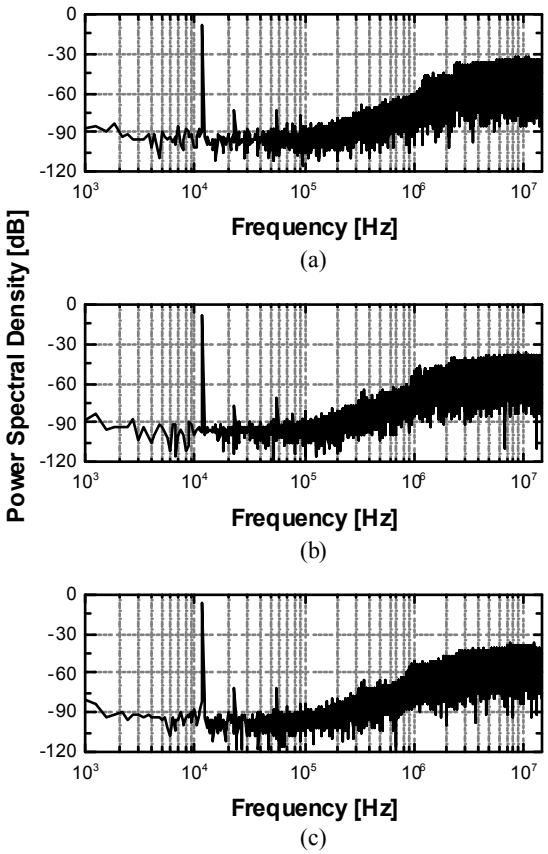

Fig. 8. Measured dynamic performance with power supplies of 1.62V (a), 1.8V (b), and 1.98V (c).

signal. Upper and lower sides of the circuit are the first and second integrators of the modulator, respectively.

Notice that sharing an amplifier between adjacent stages often degrades linearity of the ADC due to residual charge stored on the input parasitic of the amplifier [8]. However, this work does not suffer from the effect of residual charge. When INV1 is used to set the bias current, its input is shorted to a common-mode voltage for input sampling. This resets INV1 and removes residual charge on its input parasitic.

With a sampling frequency (F_S) of 20MS/s, the required DC gain and unity-gain frequency to achieve 10-bit resolution are 40dB and 150MHz, respectively, with a maximum load of 45fF. Design parameters are summarized in Table I. The worst case DC gain and unity-gain frequency are 40.5dB and 142MHz, respectively, and the amplifier draws a maximum current of 10.8μA from a 1.8V supply.

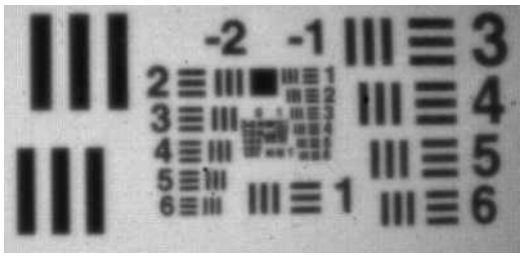

Fig. 9. Sample image with the prototype image sensor.

The amplifier noise, especially 1/f noise of the input transistors, should be carefully considered to improve the ADC's noise performance beyond 12-bit or higher. Chopping or auto-zeroing technique as in [11] can be employed to minimize the noise. In addition, compared to conventional inverters, thermal noise generated from the additional transistors (MN and MP) needs to be suppressed in order not to limit the noise performance.

IV. Experimental Results

A 384 x 200 image sensor is fabricated in a 0.18-μm 1P4M CMOS image-sensor (CIS) technology to evaluate the ADC performance. Each pixel column is read by one incremental delta-sigma ADC, which occupies an area of 0.002 mm^2. The decimation filter employing a 2nd-order cascade of integrator topology is similar to the one proposed in [11] and is shared by the 16 modulators due to the limited die space. The total capacitance of the ADC is 0.21 pF and this is mainly determined by noise performance. The die micrograph and single ADC layout are shown in Fig. 5. Fig. 6 shows the measured dynamic performance for an 11.3 kHz input sinusoidal signal. The measured SNDR for 156.25 kHz and 78.125 kHz signal bandwidth with a F_S of 20MS/s are 57.7 dB and 62.3 dB, respectively. The resulting ENOB, which is

TABLE III

PERFORMANCE SUMMARY

Technology	0.18μm 1P4M CMOS Image-sensor_
Supply	1.8 V
Resolution	10 Bit
Sampling Rate	20 MS/s
Bandwidth	156.25 kHz (OSR = 64) 78.125 kHz (OSR = 128)
SNDR @ Fin=11.3kHz	57.7 dB (OSR = 64) 62.3 dB (OSR = 128)
ENOB	9.3 Bit (OSR = 64) 10.1 Bit (OSR = 128)
DNL	+0.22 / -0.2 LSB
INL	+0.71 / -0.89 LSB
Active Area	0.0018656 mm^2
Total Power Consumption	0.0295 mW
FOM	151 fJ/Conv. Step (OSR = 64) 177 fJ/Conv. Step (OSR = 128)

calculated as (SNDR-1.76)/6.02, are 9.3 bits and 10.1 bits, respectively. The measured static performances are shown in Fig. 7. The differential nonlinearity (DNL) and integral nonlinearity (INL) are less than +0.22/-0.2 and +0.71/-0.89 LSB, respectively. Fig. 8 shows the measured dynamic performances over different supplies. The measured SNDR for the power supplies of 1.62V, 1.8V, and 1.98V are 58.2 dB, 57.7 dB and 56.7 dB, respectively. The total power consumption of the ADC is 29.5 μW from a 1.8 V supply. Since the ADC size is one of the most important specifications for CMOS image sensors, the FOM_A, which is defined by FOM·Area [J·mm^2/Conv-step], of recently published delta-sigma ADCs is compared in Table II. The ADC achieves an FOM_A that is comparable to the state-of-the-art delta-sigma ADCs implemented in more advanced technologies. Fig. 9 shows a sample image taken by the prototype image sensor and the ADC performance is summarized in Table III.

V. Conclusion

A low-power, small-size 10-bit incremental delta-sigma ADC for CMOS image sensor has been proposed and fabricated in a 0.18-μm CMOS image-sensor technology. The ADC saves power and die area by sharing a self-biasing amplifier and using the proposed level-shifting technique to perform signal summation. The ADC occupies a die area of 0.002mm^2 and dissipates 29.5μW from a 1.8-V supply. Operating at 20MS/s, the measured SNDR with 156.25kHz and 78.125kHz signal bandwidth are 57.7dB and 62.3dB, respectively, for an 11.3kHz input signal. The measured DNL and INL are less than +0.22/-0.2 and +0.71/-0.89 LSB, respectively.

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