# Optimal Design of Reversible Parity Preserving New Full Adder / Full Subtractor

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*Abstract*—**The widely using CMOS technology implementing with irreversible logic will hit a scaling limit beyond 2020 and the major limiting factor is increased power dissipation. The irreversible logic is replaced by reversible logic to decrease the power dissipation. The devices implemented with reversible logic gates will have demand for the upcoming future computing technologies as they consumes less power. Reversible logic has applications in Low Power VLSI, Quantum Computing, Nanotechnology and Optical computing. This paper proposes the design of a optimal fault tolerant Full adder/ Full subtractor. For this logic circuit input parity and output parity is same hence it is called parity preserving circuit. The proposed method require less complexity, less hardware, minimum number of gates, minimum number of garbage inputs and minimum number of constant inputs than existing methods.**

*Index Terms*—**Reversible Logic, Quantum computing, Fault Tolerant, Full Adder, Full Subtractor**

## I. INTRODUCTION

Over the last few years, reversible logic has been extensively used in numerous technologies such as DNA computing, Bio-informatics, Quantum computing and Nanotechnology. In reversible logic bit loss is recovered by unique input-output mapping where in conventional logic it is not possible. It is one of distinct feature of reversible logic. In reversible logic the input pattern is recovered from its output pattern but it fails conventional logic. In 1961, the research of R. Landauer illustrated that the amount of energy dissipated for every information bit loss is at least kTln2 joules, where k is Boltzmann constant and T is temperature at which system operation is performed [1]. The amount of energy which is dissipated due to one bit information loss is very small. But in high speed computational works the number of information bits is more. Then the heat dissipation is also more. This dissipation affects the performance and reduces the lifetime of system. In 1973, Bennet demonstrated that kTln2 energy will not be dissipated if the inputs are able to recover from its output [2]. Hence the power dissipation will be zero if a network contains only reversible logic gates. The optimization parameters for the synthesis of reversible logic circuit are

1. Minimum number of gates
2. Minimum quantum cost
3. Minimum number of constant inputs
4. Minimum number of garbage outputs
5. Minimum delay

Also direct fan-out is not allowed in the synthesis of reversible logic gates because one-to-many concept is not reversible. By using additional reversible logic gates the fan-out can be achieved. The synthesis of reversible logic is different from the conventional logic [3]. First, the reversible circuit should not have fan-out i.e., the output of any gate is connected as input to any gate once only. Secondly, the input output patterns have one to one correspondence. Lastly, the circuit must be acyclic. In addition to these a circuit is called reversible if the outputs are applied at the output then inputs are reproduced at the input i.e., we are reproducing the inputs from outputs. The fault tolerant reversible gates are special gates in reversible gates. the fault tolerant gates satisfies the property of parity preserving i.e., the parity of input and output is same. A logic block is called parity preserving if every gate in that is parity preserving [4]. If a logic block is implemented with fault tolerant gates then those gates will not require extra circuitry to check errors which occur in computation or communication.

Addition is one of the essential operation in multiplication and division algorithms. It plays a vital role in many applications like DSP processors, Micro processors and in computing devices. Hence, it is required to design fast adder. This paper presents a novel design of reversible optimized fault tolerant Full adder/ Full subtractor. This paper proposes an efficient approach to implement 1-bit adder which will play a vital role in future quantum computers.

The remaining paper is decomposed as follows. Section II presents basic definitions related to reversible logic circuits, fault tolerant gate, full adder and full subtractor. In section III we discuss basic reversible logic gates input output relationship and corresponding truth tables. Section IV describes the existing fault tolerant models of full adders, full adder/full subtractor. The section V proposes an optimal model on full adder/full subtractor. The experimental results are presented in section VI. Finally we conclude in section VII.

## II. Basic Definitions

### A. Reversible gate

Reversible gate is a digital circuit whose number of inputs and number of outputs are equal. If there are k inputs, there will be k outputs. Each input pattern has unique output pattern. This is called as one-one correspondence. It is denoted by k*k.

### B. Fault tolerant gate

Any gate which preserves the same parity between inputs and output is called as fault tolerant gate. For a k*k reversible gate fault tolerance can be analytically expressed as

$$I_1 \odot I_2 .... \odot I_N = O_1 \odot O_2 .... \odot O_N$$

The important property of a fault tolerant gate is error signal can be easily detected. Fredkin gate (FRG) [5][7], Double Feynman gate (F2G) [6], New fault tolerant gate (NFT), Islam gate (IG) [3], Modified Islam gate(MIG) are some popular fault tolerant reversible gates.

### C. Garbage output

The outputs which are used only to maintain the reversible property are called garbage outputs. These garbage outputs are unwanted outputs or not useful outputs. Garbage outputs are maintained at a rate of heavy price.

### D. Quantum cost

A reversible logic gate in a circuit can be substituted by a cascade of quantum gates. The quantum cost of reversible gate is the number of quantum gates or 2X2, 1X1 reversible gates required in its design. Reversible logic gates operate on pure logic values where as quantum gate operates on q-bits. There are many elementary quantum gates. Such as NOT gate, controlled-NOT (CNOT) gate, controlled-V gate, controlled-V+ gate. NOT gate performs inversion of a single q-bit. Controlled-NOT gate denoted by CNOT gate performs inversion of the input q-bit only if control q-bit is 1. Controlled-V gate is also called as square root of NOT(SRN) gate. Two consecutive V operations is equal to inversion operation. Controlled-V+ gate is also called as square root of NOT gate. The quantum costs of various gates are FRG is 5, F2G is 2, NFT is 5, IG and MIG is 7.

### E. Quantum Gate Complexity

Each reversible logic gate is build using elementary quantum gates such as NOT, CNOT, Controlled-V and Controlled-V+ gates. The number of elementary quantum gates required to synthesize a reversible logic gate is called as quantum gate complexity. Controlled-V gate (SRN) and its hermitian i.e., controlled-V+ gate are similar gates. Let $\alpha$ be the complexity of a NOT gate calculation, $\beta$ be the complexity of a CNOT gate and $\gamma$ be the complexity of SRN and its Hermitian. A Fredkin gate has 3 Controlled-V & V+ gates and 4 CNOT gates. So the quantum gate complexity of Fredkin gate is $4\beta + 3\gamma$.
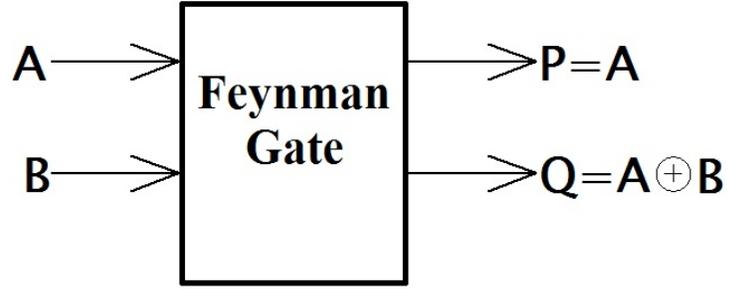


Fig. 1. Feynman gate

### F. Delay

The delay of a reversible logic gate is measured in terms of unit delay denoted by '$\Delta$'. '$\Delta$' represents the delay of a 1*1 or 2*2 elementary quantum gate. Such as NOT, CNOT, Controlled-V gate, controlled-V+ gate. Hence the logical depth of the circuit is necessary for measuring delay. For Fredkin gate delay is $5\Delta$.

### G. Area

The total area of a reversible logic circuit is the sum of areas occupied by individual reversible logic gates. In a reversible logic circuit, if there are n reversible logic gates having areas $a_1, a_2, a_3, ........, a_n$ then the total area occupied by reversible logic circuits is

$$A = \sum a_i$$

### H. Power

The total power of a reversible logic circuit is the sum of power of each reversible logic gate. In a reversible logic circuit, there are n reversible logic gates with powers $p_1, p_2, p_3, ........, p_n$ then total power of the reversible logic circuit is given by

$$P = \sum p_i$$

## III. Basic Reversible Logic Gates

There are many reversible gates available in literature. Among them few important gates are Feynman Gate (FG), Feynman Double Gate (F2G), Fred kin Gate (FRG), Toffoli Gate (TG), and Peres Gate (PG).

### A. Feynman gate

Feynman gate[6] is one of the basic reversible logic gate with 2 inputs and 2 outputs, Also called as 2*2 gate, depicted in Fig. 1. along with truth table in Table I. The inputs are denoted by I (A, B) and the outputs are denoted by O (P, Q). The outputs are given by

$$P = A \ ; Q = A \oplus B \ ;$$

Feynman gate is called as a copying gate. The quantum cost of a Feynman gate is one.

TABLE I
TRUTH TABLE OF FEYNMAN GATE

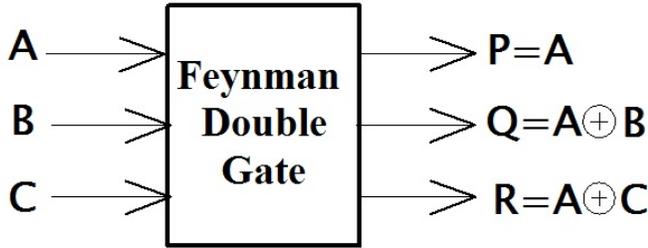| Inputs | | Outputs | |
|---|---|---|---|
| A | B | P | Q |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |



Fig. 2. Feynman Double gate

### B. Feynman Double Gate

Feynman Double gate [6] is also one of the basic reversible logicgate with 3 inputs and 3 outputs also represented as 3*3 gate. It is depicted in Fig. 2. along with truth table in Table II. The inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, R).The relation between inputs and outputs are given by

$$P = A \; ; \; Q = A \oplus B \; ; \; R = A \oplus C \; ;$$

Quantum cost of a Feynman double gate is 2

### C. Toffoli Gate

Toffoli gate [5][9] is also one of the basic reversible logic gates with 3 inputs and 3 outputs. It also called as 3*3 gate. It is depicted in Fig. 3. along with truth table in Table III. For a toffoli gate, the inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, R).The relationship between inputs and outputs is

TABLE II
TRUTH TABLE OF DOUBLE FEYNMAN GATE

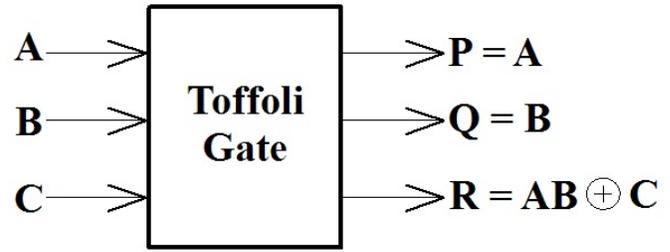| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |



Fig. 3. Toffoli gate

TABLE III
TRUTH TABLE OF TOFFOLI GATE

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

$$P = A \; ; \; Q = B \; ; \; R = AB \oplus C \; ;$$

The quantum cost of a Toffoli gate is 5

### D. Fredkin Gate

Fredkin gate [5][7] is also one of the basic gate of reversible logic gate with 3 inputs and 3 outputs and denoted by 3*3 gate. It is depicted in Fig. 4. along with truth table in Table IV. The inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, and R). The relationship between inputs and outputs is given by

$$P = A \; ; \; Q = \bar{A}B \oplus AC \; ; \; R = \bar{A}C \oplus AB \; ;$$

For Fredkin gate the quantum cost is 5.

### E. Peres Gate

Peres gate[8] is also one of the basic reversible logic gate with 3 inputs and 3 outputs also denoted as 3*3 gate. It is
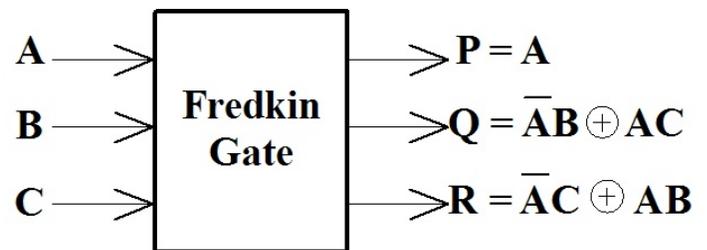


Fig. 4. Fredkin Gate

TABLE IV
TRUTH TABLE OF FREDKIN GATE

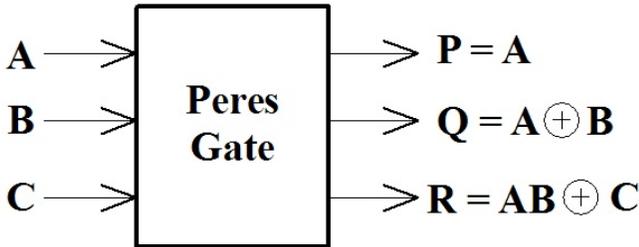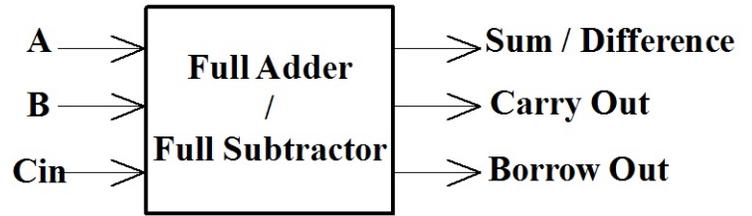| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |



Fig. 5. Peres Gate



Fig. 6. Symbol Of Full Adder / Full Substractor

TABLE VI
TRUTH TABLE OF FULL ADDER / FULL SUBTRACTOR

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| A | B | $C_{in}$ | Sum/ Difference | $C_{out}$ | $B_{out}$ |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

depicted in Fig. 5. along with truth table in Table V. The inputs are denoted by I (A, B,C) and outputs are denoted by O(P, Q, R). The relationship between inputs and outputs is given by

$$P = A \; ; \; Q = A \oplus B \; ; \; R = AB \oplus C \; ;$$

For Peres gate the quantum cost is 4

## IV. EXISTING WORK

Many fault tolerant reversible logic full adder structures are proposed earlier [10-14]. A structure proposed in [10] is implemented with feynman double and fredkin gates. In that paper first they implemented half adder/half subtractor then they implemented full adder/full subtractor using half adder/half subtractor and fredkin gate. In [11], a new gate parity conserving toffoli gate (PCTG) is designed and using

TABLE V
TRUTH TABLE OF PERES GATE

| Inputs | | | Outputs | | |
|---|---|---|---|---|---|
| A | B | C | P | Q | R |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

that gate they implemented full adder structure. One PCTG gate contains one Feynman double and one fredkin gate. To implement one full adder two PCTG and two Feynman double gates are required. In similar way many structures are proposed in [12-14]. But by studying above said papers it is observed that they requires more number of gates, high garbage, many constant inputs and high quantum cost. Also many of the papers implement only full adder. So here a model is proposed with best performance.

## V. PROPOSED WORK

In every digital circuit the basic components are N-Bit Adders and N-Bit Multipliers. In the above said components the basic element is 1-Bit Adder. If we worked to implement 1-Bit Adder efficiently then it indirectly helps for the optimistic design of any Digital circuit. This paper proposes a circuit which works as a Full Adder and full Subtractor. Its symbol is shown Fig. 6. and Truth Table is shown in Table VI.

A full adder is a combinational circuit that adds 3 input bits and produces 2 outputs. In the 3 input bits 2 bits are data bits and other bit is previous stage carry. The 3 input variables are denoted by A, B and $C_{in}$. The outputs sum and carry are denoted by 'S' and '$C_{out}$'. The mathematical equation representing the full adder is A+B+$C_{in}$. A full subtractor is a combinational circuit that subtracts 2 input bits from first input and produces 2 outputs. In the 3 input bits 2 bits are data bits and other bit is present stage borrow. The 3 input variables are denoted by A, B and $C_{in}$( for convenience purpose present stage borrow is denoted by $C_{in}$ ). The outputs Difference

and Borrow are denoted by 'D' and 'B$_{out}$'. The mathematical equation represents full subtractor is A-B-C$_{in}$. The boolean expressions of Full Adder / Full Subtractor are

$$\text{Sum / Difference} = A \oplus B \oplus C_{in}$$
$$\text{Carry out } (C_{out}) = (A \oplus B)C_{in} + AB$$
$$\text{Borrow out } (B_{out}) = (A \odot B)C_{in} + \overline{A}B$$

The carry out and borrow out expressions can be modified and rewritten as

$$\text{Carry out } (C_{out}) = (A \oplus B)C_{in} \oplus AB$$
$$\text{Borrow out } (B_{out}) = (A \odot B)C_{in} \oplus \overline{A}B$$

Reversible logic adder circuits which are implemented earlier by several authors are not fault tolerant (Peres gate) i.e., the parity of input and parity of output is not same. This paper describes the fault tolerant Full adder/ Full subtractor with minimal garbage outputs and constants inputs.To implement the full adder/subtractor we are using 3 Feynman double gates and one Fredkin gate.

*A. Design of optimal fault tolerant Full adder / Full subtractor*

The circuit diagram of optimal fault tolerant Full adder / Full subtractor is shown in Fig. 7. It contains F2G-1, F2G-2, F2G-3 and one Fredkin gate. For the first Feynman double gate (F2G-1) the inputs are B and A and one constant input '0'. By using this first Feynman double gate we are duplicating the B' input and A⊕B is generated. One 'B' output act like garbage output (G1). For second Feynman double gate (F2G-2) the inputs are 'C' and 2 constant inputs '0'.

The second Feynman double gate (F2G-2) is used to triplicate the C$_{in}$. For this purpose C$_{in}$,'0','0' are applied as inputs to second Feynman double gate (F2G-2) and it produces all outputs as C$_{in}$. Among three outputs one of the C$_{in}$ acts like garbage output (G2).

For third Feynman double gate (F2G-3), the inputs are A⊕B i.e., output of first Feynman double gate (F2G-1), C$_{in}$ i.e., output of second Feynman double gate (F2G-2) and one constant input '0' then the outputs are A⊕B (garbage output G3), A⊕B⊕C$_{in}$ i.e., SUM / DIFFERENCE and A⊕B.

The A⊕B (output of third Feynman double gate (F2G-3)), C$_{in}$ (output of second Feynman double gate (F2G-2)), B ( output of first Feynman double gate (F2G-1)) are applied as inputs to the Fredkin gate. The outputs are A⊕B (garbage output G4), BORROW out and CARRY out. The symbol of Optimized Parity Preserving Full Adder / Full Substractor is shown in Fig. 8.

The following circuit also satisfies the reversibility principle i.e., explained in Fig. 9. In the diagram two OPPFAFS are considered. For OPPFAFS-1 inputs are applied. The outputs of OPPFAFS-1 are connected to OPPFAFS-2 across output. The
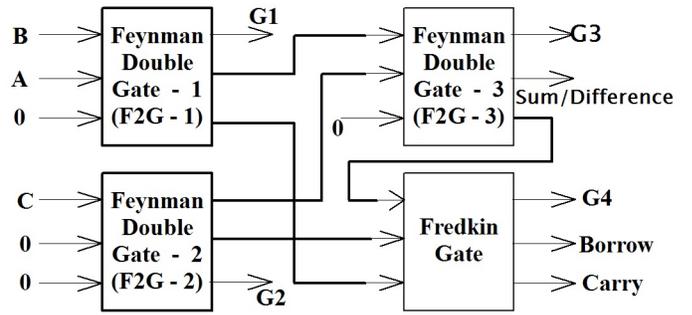


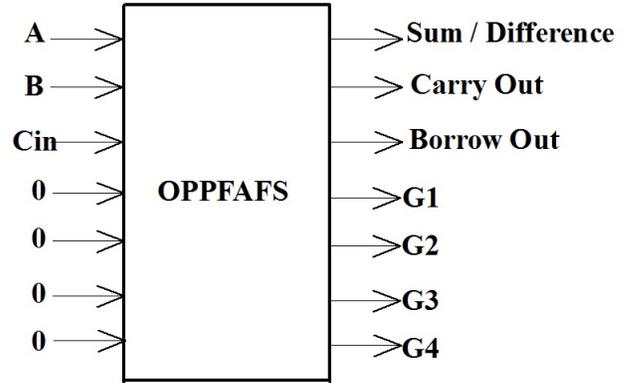Fig. 7. Optimized Parity Preserving Full Adder / Full Substractor



Fig. 8. Symbol of Optimized Parity Preserving Full Adder / Full Substractor

OPPFAFS-2 going to reproducing inputs. Hence it satisfies reversibility principle.

## VI. PERFORMANCE EVALUATION

The proposed model is simulated in CADENCE gpdk 180nm Technology in digital domain and obtained suitable results as shown in Fig. 10. The performance parameters like power, gate count, garbage outputs, constant inputs and quantum cost for proposed model and existing model are shown in Table VII. In [10], fault tolerant Full adder/ Full Subtractor
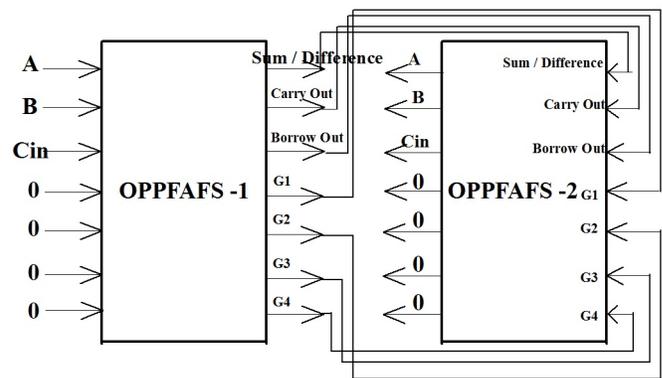


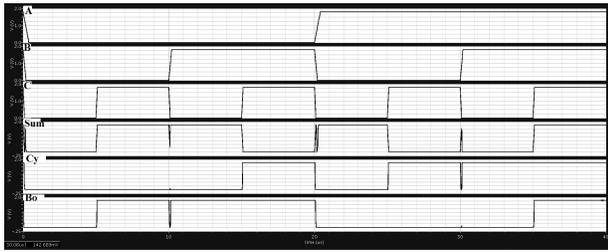Fig. 9. Block diagram showing reversibility

Fig. 10. Results of Optimized Parity Preserving Full Adder/Full Substractor

is proposed and there is an improvement of 50% power, 50% gate count, 63% garbage outputs, 55% constant inputs and 56% quantum cost than the proposed model. In [11], only fault tolerant Full adder is proposed and there is an improvement of 20% power, 33% gate count, 33% garbage outputs, 20% constant inputs and 40% quantum cost than the proposed model. Hence, the proposed model of full adder/full subtractor is giving better performance than mentioned existing models.

## VII. CONCLUSION

This paper focus mainly on implementation of a model which can be operated as full adder as well as full subtractor with better performance. Here a structure is proposed with parity preserving gates which reduces testing hardware. The reversible logic concept work efficiently if number of garbage outputs, constant inputs and quantum cost is low. The power dissipation is zero if the reversible logic circuits are implemented with quantum gates. If we do that then we can save power, money as well as nature.

TABLE VII
COMPARATIVE ANALYSIS OF VARIOUS STRUCTURES

| Fault Tolarent Full Adder /Full Subtractor | Power | Gate Count | Garbage Outputs | Constant Inputs | Quantum Cost |
|---|---|---|---|---|---|
| [10] Full Adder/ Subtractor | $41.21\mu$W | 3 FRG 5 F2G | 11 | 09 | 25 |
| [11] Full adder Only | $25.62\mu$W | 2 FRG 4 F2G | 06 | 05 | 18 |
| Proposed | $20.22\mu$W | 1 FRG 3 F2G | 04 | 04 | 11 |

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