Design And Synthesis Of Combinational Circuits Using Reversible Decoder In Xilinx

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***Abstract*—Reversible logic is the emerging field for research in present era. The aim of this paper is to realize different types of combinational circuits like full-adder, full-subtractor, multiplexer and comparator using reversible decoder circuit with minimum quantum cost. Reversible decoder is designed using Fredkin gates with minimum Quantum cost. There are many reversible logic gates like Fredkin Gate, Feynman Gate, Double Feynman Gate, Peres Gate, Seynman Gate and many more. Reversible logic is defined as the logic in which the number output lines are equal to the number of input lines i.e., the n-input and k-output Boolean function F(X1, X2, X3,…, Xn) (referred to as (n, k) function) is said to be reversible if and only if (i) n is equal to k and (ii) each input pattern is mapped uniquely to output pattern. The gate must run forward and backward that is the inputs can also be retrieved from outputs. When the device obeys these two conditions then the second law of thermo-dynamics guarantees that it dissipates no heat. Fan-out and Feed-back are not allowed in Logical Reversibility. Reversible Logic owns its applications in various fields which include Quantum Computing, Optical Computing, Nano-technology, Computer Graphics, low power VLSI Etc., Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption. The comparative study in terms of garbage outputs, Quantum Cost, numbers of gates are also presented. The Circuit has been implemented and simulated using Xilinx software.**

***Keywords-Quantum Cost, Reversible Gates, Garbage Outputs, Number of Gates*.**

I. INTRODUCTION

In present VLSI Technology, Power Consumption has become a very important factor for consideration. By using Reversible Decoder for designing Combinational circuits power consumption is reduced to an optimum when compared to conventional decoder based combinational circuits. Reversible Logic finds its own application in Quantum computing, Nano- technology, optical computing, computer graphics and low Power VLSI. Ralf Launduer [1] told that heat dissipation in circuits is not because of the process involved in the operation, but it is due to the bits that were erased during the process. He introduced that losing of a single bit in the circuit causes the smallest amount of heat in the computation which is equal to KTln2 joules where K is Boltzmann constant and T is Temperature. The amount of heat dissipated in simple circuits is very small but it becomes large in the complex circuits which imply propagation delay also. Later in 1973 C. H. Bennett [2] described that the Power dissipation due to the bit loss can be overcome if each and every computation in circuit was carried out in reversible manner. Quantum networks are designed of quantum logic gates. As each gate perform a unitary operation, KTln2 Joules energy dissipation wouldn't occur if the computation is carried out in reversible manner. Thus computation done in reversible manner doesn't require erasing of bits. The amount of heat dissipated in the system holds a direct relationship to the number of bits erased or lost during the computation.

II. CONCEPT

The Reversible Logic involves the use of Reversible Gates consists of the same number of inputs and outputs i.e., there should be one to one mapping between input vectors and output vectors. And they can be made to run backward direction also. Certain limitations are to be considered when designing circuits based on reversible logic (i) Fan out is not permitted in reversible logic and (ii) Feedback is also not permitted in reversible logic. In Reversible logic using outputs we can obtain full knowledge of inputs. Reversible logic conserves information. Some cost metrics like Garbage outputs, Number of gates, Quantum cost, constant inputs are used to estimate the performance of reversible circuits. Garbage outputs are the extra outputs which help to make inputs and outputs equal in order to maintain reversibility. They are kept alone without performing any operations. Number of gates count is not a good metric since more number of gates can be taken together to form a new gate. Quantum Cost is the number of elementary or primitive gates needed to implement the gate. It is nothing but the number of reversible gates (1×1 or 2×2) required to construct the circuit. Delay is one of the important cost metrics. A Reversible circuit design can be modeled as a sequence of discrete time slices and depth is summation of total time slices. In Digital Electronics the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various proposals are given to design of combinational and sequential circuits in the undergoing research.

In this paper, the design of different combinational circuits like binary comparator, Full adder, Full subtractor, Multiplexer circuits using Reversible Decoder is proposed with optimum Quantum cost.

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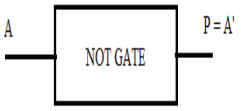
III. REVERSIBLE LOGIC GATES

The basic Reversible Logic Gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

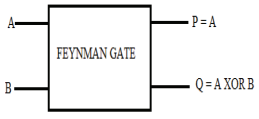
1. *NOT GATE:* The NOT GATE is the simple Reversible Logic gate. It is 1×1 Reversible Logic Gate with the quantum cost zero. The Not gate simply shifts the complementary of the input to output as shown in the figure1. It is the basic primitive gate which may involve in construction of reversible logic gate, thus owing its own importance in determining the quantum cost of designed Reversible logic gate.



A	P
0	1
1	0

Fig. 1 NOT Gate and its Truth Table

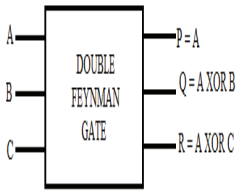
2. *FEYNMAN GATE (FG):* Feynman gate is a 2×2 reversible gate as shown in below figure2. The Feynman gate is also called as CNOT gate i.e., controlled NOT gate. The Feynman gate is used to duplicate of the required outputs since Fan-out is not allowed in reversible logic gates. The Quantum Cost of FG is 1. This is also the primitive gate owing its importance in determining quantum cost metric.



A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 2 Feynman Gate and its Truth Table

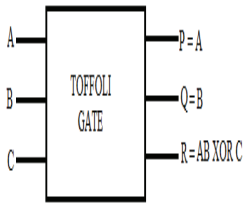
3. *DOUBLE FEYNMAN GATE (DFG):* Double Feynman Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure3. The quantum cost of DFG is 2. This gate can also be used for duplicating outputs.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig.3.Double Feynman Gate and its Truth Table

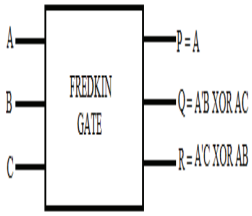
4. *TOFFOLI GATE (TG):* Toffoli Gate is 3×3 reversible gate. The outputs are defined as shown in the below figure4. The Quantum Cost of TG is 4.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Fig.4 Toffoli Gate and its Truth Table

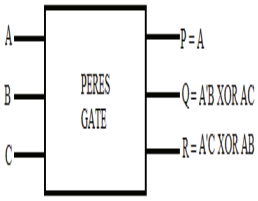
5. *FREDKIN GATE (FDG):* Fredkin Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure4. The Quantum Cost of FDG is 5. This paper mainly surrounds around Fredkin gate.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig.5 Fredkin Gate and its Truth Table

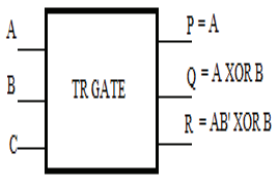
6. *PERES GATE (PG):* Peres Gate is a is a 3×3 reversible gate. The outputs are defined as shown in the below figure6. The Quantum Cost of PG is 4.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig.6 Peres Gate and its Truth Table

7. *TR GATE:* TR Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure7. The quantum cost of TRG gate is given by 4.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

Fig.7 TR Gate and its Truth Table

IV. BASIC GATES USING REVERSIBLE GATES

Considering our circuit requirements we need to design AND gate and OR gate using reversible gates. Here we used fredkin gate to design AND and OR gates as shown in figure8. Importance is given to fredkin gate because it gives optimistic performance at less Quantum Cost for designing AND and OR gates.

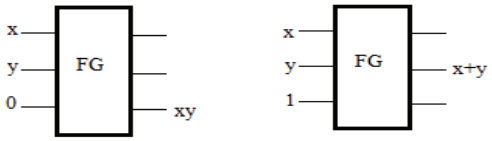


Fig.8 AND Gate using fredkin and OR Gate using fredkin

V. EXISTING METHOD

The Design of Combinational and Sequential Circuits has been ongoing in research. Various proposals are given for the design of combinational circuits like adders, subtractors, multiplexers, decoders etc., in the existing method the author has given a novel design of 4x16 decoder whose Quantum Cost is less than the previous design. Replacing fredkin gates for designing 2×4 decoder reversible gates like peres gate, TR gate, NOT gate and CNOT gate are used as shown in figure9. The whole design is done using Fredkin, CNOT, Peres gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 4x16 decoder are 18 in which there are 12 fredkin gates, one peres gate, one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of 4x16 decoder.

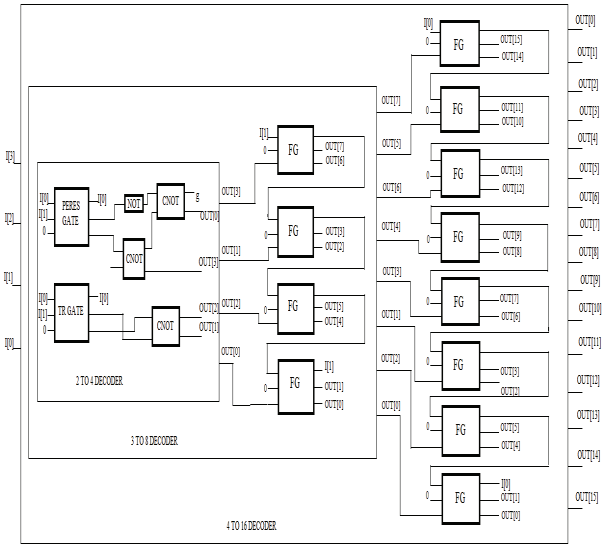


Fig 9: Circuit diagram of Reversible 4×16 decoder

VI. PROPOSED METHOD

Different Reversible Decoder circuits like 2×4, 3×8, 4×16 are designed using Fredkin Gates (mainly), Feynman gates and Peres gate. Some combinational circuits like comparator adder, subtractor, multiplexers etc., are designed using these decoders. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation.

VII. SIMULATION RESULTS OF PROPOSED CIRCUITS

1. 4×16 DECODER

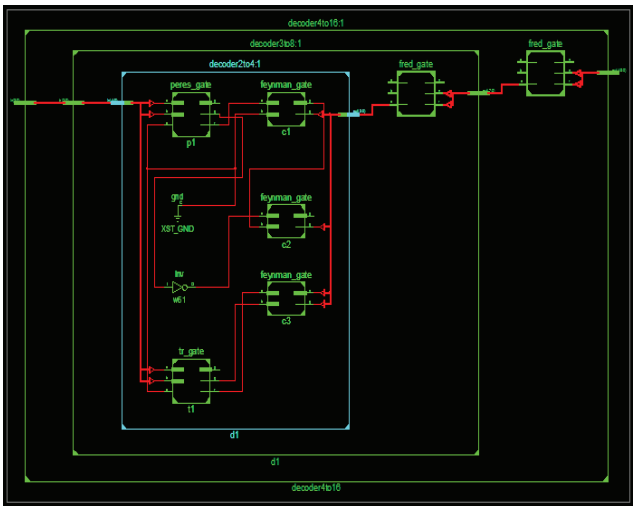
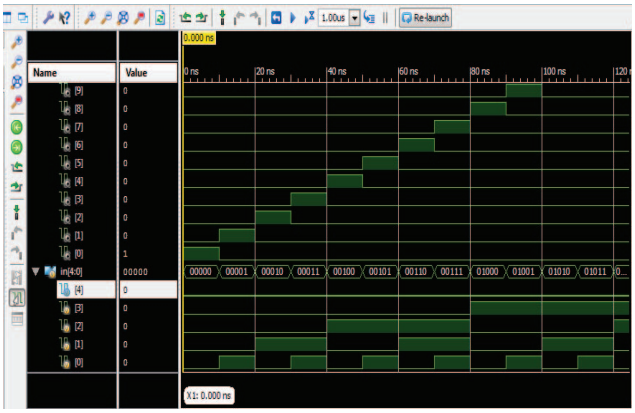


Fig.10 RTL Schematic of 4×16 reversible decoder



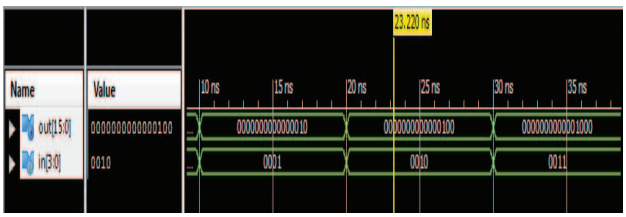


Fig.11 simulated output for 4 ×16 decoder

It is clear from the above simulated output in figure11 resembling stair case that different binary integer value is converted to associated pattern of outputs.

2. BINARY COMPARATOR

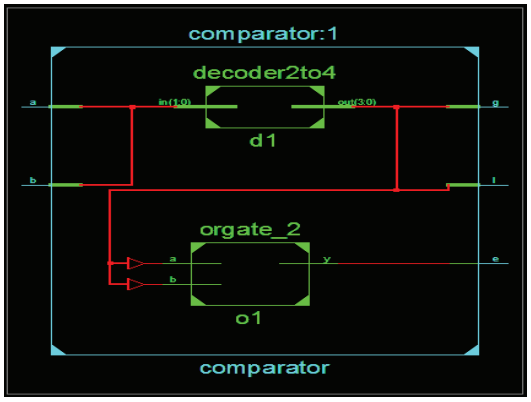


Fig.12 RTL Schematic of Binary Comparator

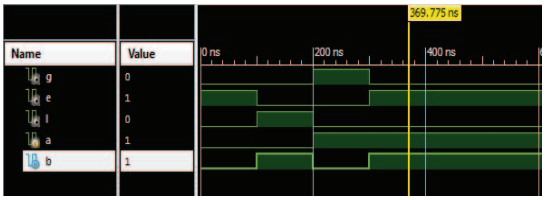


Fig.13 Simulated output for Binary Comparator

The output lines g, l, e represents Greater, Lesser, Equal respectively. The a, b lines represents the inputs. If a<b then 'l' output becomes high. If a>b then 'g' output becomes high. If a=b then 'e' output becomes high.

3. FULL ADDER/ SUBTRACTOR

The concept of duplicating one output to two outputs using Feynman gate is introduced. The second input of Feynman gate was made to 0 which drives two splitted equivalent outputs.

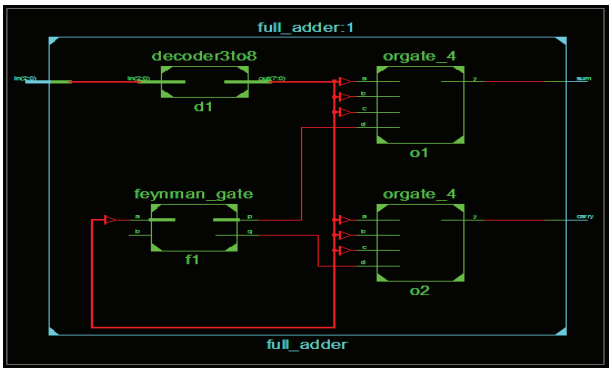


Fig 14: RTL Schematic of full adder

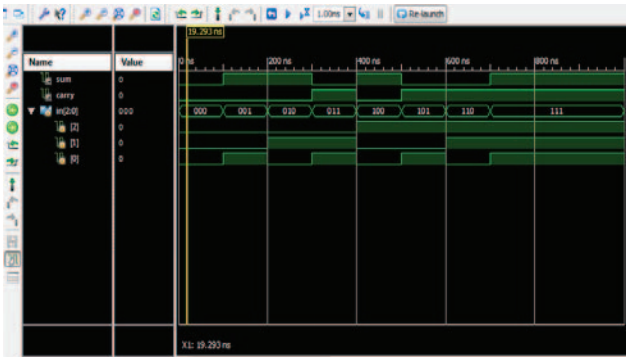


Fig.15 Simulated output for Full adder

For designing a full adder a 3 to 8 decoder and two four input OR gates are required. The min terms for SUM and CARRY are derived from output pattern of decoder. Similarly the full subtractor was also designed.

Equation for sum S=∑ (1, 2, 4, 7)
Equation for carry C=∑ (3, 5, 6, 7)
Equation for difference D=∑ (1, 2, 4, 7)
Equation for borrow B=∑ (1, 2, 3, 7)

In the above min term expressions we can observe that the same min term output of decoder drives sum and carry outputs of full adder (i.e., out[7] of decoder output pattern). Since Fan-out is not allowed in reversible logic, the Feynman gate is used to duplicate outputs. Similarly for full subtractor outputs of decoder (i.e., out[1], out[2] and out[7]) are duplicated. By using this full adder a 4 bit full adder/subtractor is designed. The simulated output is shown in figure15. To design 4-bit full adder/subtractor circuit four full adders are required. The Cin input drives the first full adder. If Cin is given with low input 4-bit addition is performed and if Cin is given with high input the 4-bit subtraction in the form of 1's complement addition is performed.

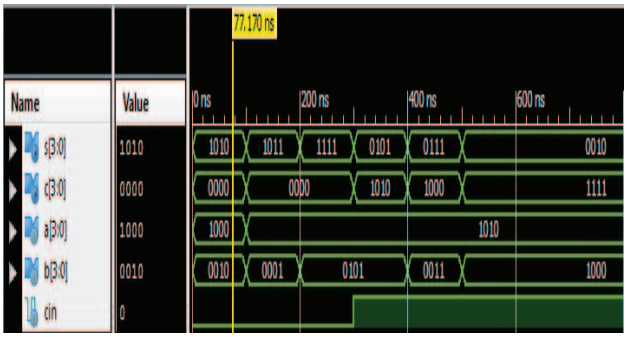


Fig.16 Simulated output for 4-bit adder/subtractor

4. MULTIPLEXER

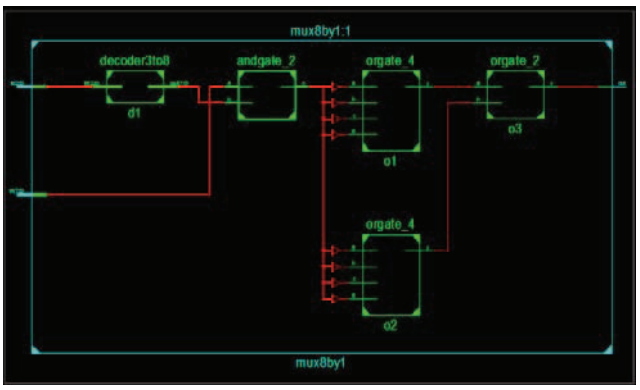


Fig.17 RTL Schematic of 8×1 multiplexer

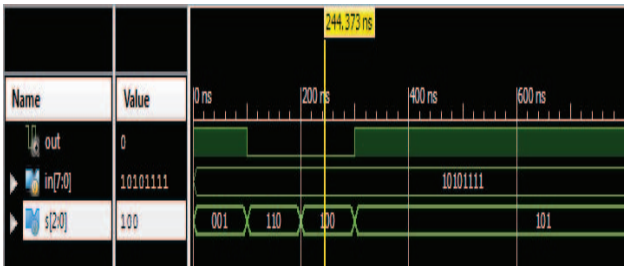


Fig.18 Simulated output of 8×1 multiplexer

To design a multiplexer using reversible decoder, reversible 2 input AND gates, 2 input OR gates are required. The 2 input AND Gate and OR gate are designed using Fredkin gate. By using these designed gates we can improve those gates to the required number of input gate. Each output line from decoder is driven to 2 input AND gate along with multiplexer input. The outputs of all AND gates are made to drive to that particular input OR gate. The input binary integer values act as the selection lines. Similarly by using 4×16 decoder a 16×1 multiplexer is designed. The RTL Schematic and the simulated outputs of 16×1 multiplexer are shown in figure19.

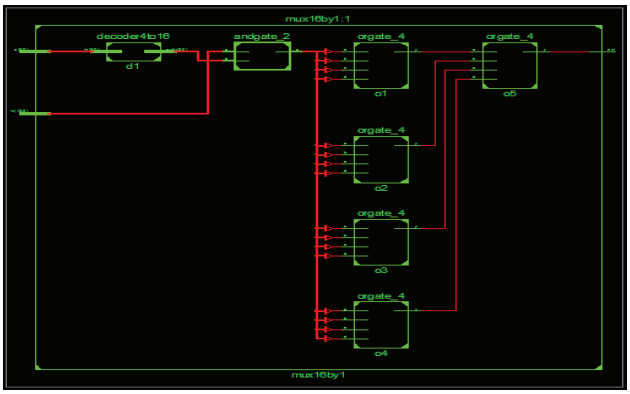


Fig.19 RTL Schematic of 16×1 multiplexer

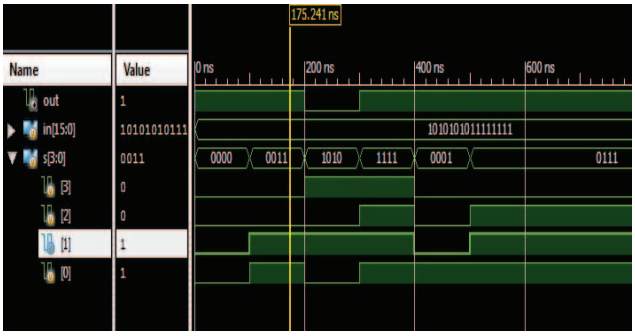


Fig.20 Simulated result for 16×1 multiplexer

VII. COMPARATIVE STUDY

The combinational circuits designed using reversible decoder are analyzed in terms of Quantum cost and Garbage outputs.

CIRCUIT	QUANTUM COST	GARBAGE OUTPUTS
2 TO 4 DECODER	11	3
3 TO 8 DECODER	31	4
4 TO 16 DECODER	71	5
BINARY COMPARATOR	16	5
FULL ADDER	61	12
FULL SUBTRACTOR	63	12
4×1 MULTIPLEXER	46	17
8×1 MULTIPLEXER	75	39

VIII. CONCLUSION

In this paper, different combinational circuits like full adder, full subtractor, multiplexer, comparator circuits constructed using reversible decoder are designed. These circuits are designed for minimum quantum cost and minimum garbage outputs. The method proposed for designing the decoder circuit can be generalized. For example, a 3×8 decoder can be designed using a 2×4 decoder followed by 4 fredkin gates, Similarly a 4×16 decoder can be designed using 3×8 decoder followed by 8 fredkin gates .The concept of duplicating the single output to required number of outputs is utilized to overcome the fan-out limitation in reversible logic circuits. This method of designing combinational circuits helps to implement many digital circuits with better performance for minimum quantum cost.

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