Voltage Unbalance Compensation by a Grid Connected Inverter Using Virtual Impedance and Admittance Control Loops

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***Abstract*— In this paper, voltage unbalance compensation using DG interfacing inverter is proposed. By using this control method, the DG not only can inject generated power to the grid, but also can compensate the unbalance voltage of the Point of Common Coupling (PCC). A compensation scheme based on negative sequence virtual impedance or admittance is proposed. The control method is designed in stationary reference frame and is based on Proportional-Resonance (PR) controller. The compensation is achieved by using only local measurement. The simulation results in Matlab/Simulink verify the effectiveness of the proposed control method.**

Keywords—distributed generating (DG); voltage unbalance; power quality compensation; virtual impedance, virtual admittance

I. INTRODUCTION

Trend of using Renewable Energy Sources (RESs) has been increased due to extinction and pollution of conventional fuels [1],[2]. Microgrids have been emerged for increasing the use of distributed generation [3]. Power electronics devices are required for integrating these energy resources to the grid or supplying local loads. Since, the output voltages of the RESs are in DC form or should be rectified, for integration of them to the ac grids, inverters are required [4].

On the other hand, due to increasing use of nonlinear and unbalance loads, the power quality has been a concern of utility companies. Specifically, unbalance voltages can cause some problems such as malfunction of (power) electronics devices, increasing the loss and decreasing the stability of the power system [5]. Due to the mentioned problems, International Electrotechnical Commission (IEC) recommends 2% of negative sequence voltage for distributed systems [6]. Using series and parallel active power filters are proposed by researcher for compensation of unbalanced voltages and currents [7], [8].

The use of the DG interfacing inverters capacity for grid power quality enhancement has been proposed in some previous works. In other words, by proper control of the power electronics interfacing inverters not only the power generated by RESs can be injected to the grid, but also the power quality compensation can be achieved [9]. Using two series and shunt inverters is proposed in [10] where the series inverter can compensate the voltage unbalance by injecting negative sequence voltage. Compensation of unbalance current by DG interfacing inverters is also presented in [11].

Unbalance compensation approaches by using negative sequence virtual impedance and droop control are presented in [12] and [13], respectively. Using hierarchical control for power quality and voltage unbalance compensation is proposed in [14] and [15].

In [16], virtual admittance is applied for PCC voltage harmonics compensation. The method is based on local measurement and cascaded current and voltage control loops. Since this control method is applied to a single phase system, the unbalance voltage compensation is not presented. The current controller is used for both power quality enhancement and fundamental power injection. An adaptive virtual impedance scheme is also proposed for current controlled inverter in [17] for harmonics compensation. The method presented in [17 is only for current controlled inverter and

Using parallel voltage and current control loops for voltage harmonics compensation of DG interfacing inverters is proposed in [18] and [19]. In this control method, the current controller is used for power quality improvement and only a fundamental positive sequence virtual impedance loop has been used for decoupling the virtual impedance.

In this paper, the compensation of the voltage unbalance using virtual impedance and admittance by grid connected voltage source inverters is proposed. The control system is based on parallel voltage and current controllers and uses local measurements. In other words, the control method which is presented in [19] is extended for three phase systems to compensate voltage unbalance. The performance of the proposed method in compensation of PCC voltage is evaluated by simulation results which are implemented in MATLAB/Simulink.

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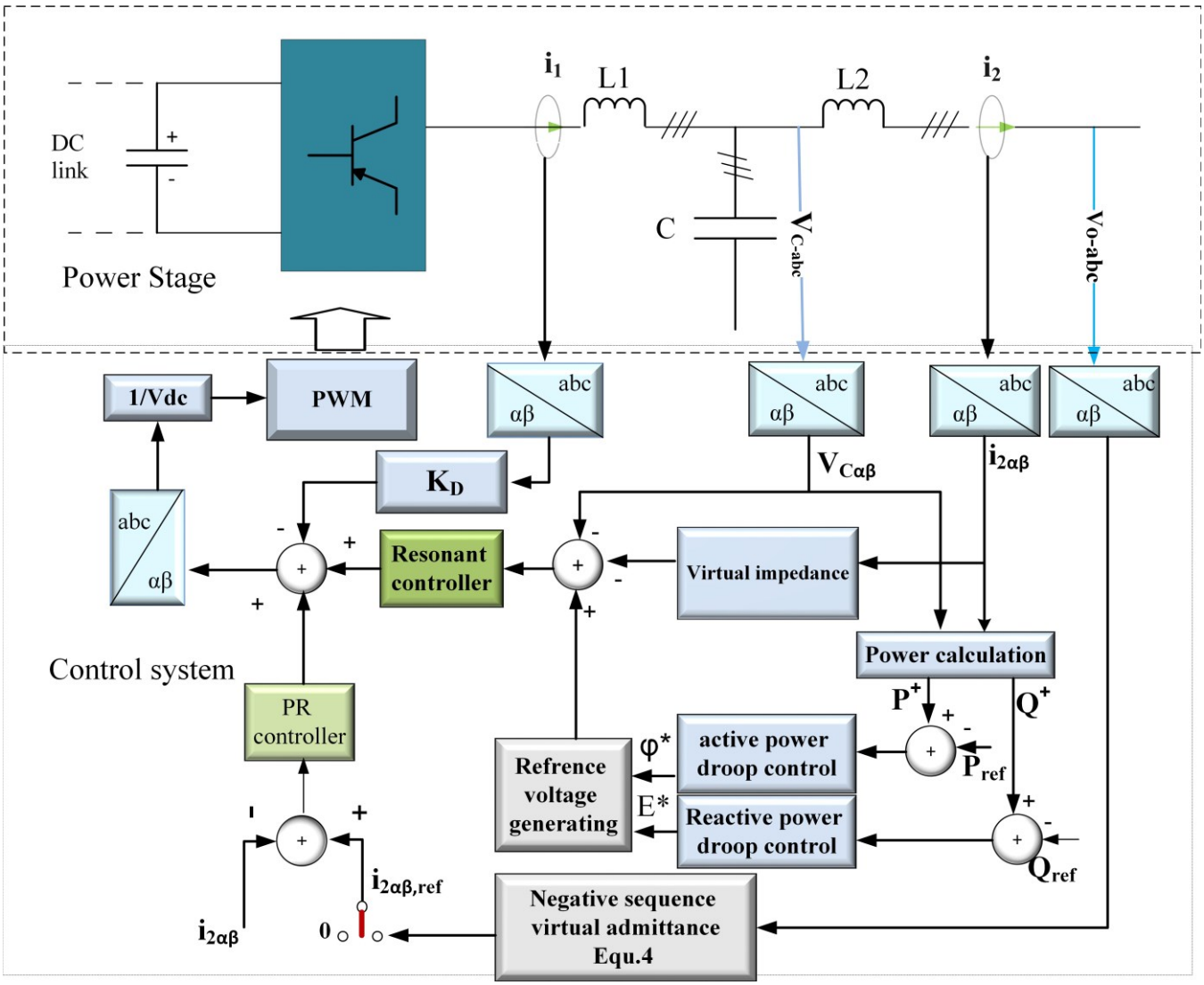


Fig. 1-The control and power stages

I. CONTROL SCHEME OF INTERFACING INVERTER

Fig.1 shows the power and proposed control stages of DG interfacing inverter. As shown in this figure, the interfacing inverter is connected to the grid via an LCL filter. Since, the control method is based on $\alpha\beta$ reference frame, the Clarke transformation is used for transforming the current and voltage variables to this stationary frame. It should be mentioned that since the system is three-wire three-phase, the zero sequence currents and voltages do not exist.

The fundamental positive sequence active and reactive powers are calculated based on the instantaneous active and reactive theory by using a low pas filter. The fundamental positive sequence voltage is generated by P- Φ and Q-E power droops control as follow [20]:

$$\varphi^* = \varphi_0 + \left(m_P (P_{ref} - P^+) + m_I \int (P_{ref} - P^+) dt \right)$$
$$E^* = E_0 + \left(n_P (Q_{ref} - Q^+) + n_I \int (Q_{ref} - Q^+) dt \right) \quad (1)$$

Where P_{ref} and Q_{ref}. are the reference active and reactive powers. The positive sequence active and reactive powers are represented by Q^+ and Q^-, respectively. The proportional and integral gains of P- φ droop coefficients are represented by m_P and m_I while the n_P and n_I are the proportional and integral gains of Q- E droop. The φ^* and E^* are the generated voltage phase angle and amplitude by active and reactive droop controls while their reference values are represented by φ_0 and E_0.

The reference voltage is compared with the capacitor voltage and after subtracting virtual impedance voltage, passes through a resonant controller. The controller is described by Eq.2:

$$G_V = \frac{2K_V\omega_b s}{s^2 + 2\omega_b s + (2\pi f)^2} \quad (2)$$

where K_V and ω_b represent the gain and band width of the resonant controller.

In this paper, the control method of inverter is based on parallel voltage and current controllers which are presented in [18] and [19]. This is extended here for three phase systems to compensate unbalanced voltages. The control method consists of three parts. The first part is the aforementioned voltage controller. The second part is current controller which is parallel with voltage controller. The controller receives a feedback of the inverter output current (i_2) and tracks reference current. The reference current ($i_{2,ref}$) can be zero; in this mode, the inverter acts like conventional inverter without any unbalanced voltage compensation. On the other hand, the reference current can be generated by virtual admittance block which will be presented in Section III. The current loop is a PR controller which is described by Eq.3.

$$G_I = K_{PI} + \frac{2K_{II}\omega_b s}{s^2 + 2\omega_b s + (2\pi f)^2} \quad (3)$$

where K_{PI} and K_{II} are proportional and integral gains of the current control, respectively.

In order to damp the renounce problem caused by using LCL filter, the inverter current is used and it passes through a proportional controller as explained in [17].

II. Power Quality Enhancement Using Virtual Impedance and Admittance

The virtual impedance consists of fundamental and negative sequence parts. Since, the current and voltage contain both negative and positive sequences; the extraction of them is required. The extraction of these components is implemented by using Second Order Generalized Integrator (SOGI) which is presented in [21].

Since the amount of feeders' resistance is not negligible in distributed systems, the fundamental inductive-resistive virtual impedance is used for decoupling the active power from the voltage amplitude and reactive power from frequency. The resistive-capacitive negative sequence virtual impedance is used for compensating the negative sequence voltage [21]. The negative sequence capacitive-resistive and positive sequence inductive-resistive virtual impedance schemes are shown in Fig. 2 where the negative and positive sequences of current ($I_{2\alpha\beta}^-$ and $I_{2\alpha\beta}^+$) should be extracted firstly. In this figure, R_V^- and R_V^+ represent the negative and positive sequences virtual resistance, respectively.

According to Fig. 2, using the capacitive virtual impedance can insert capacitor. The impedance of the capacitor is equal to

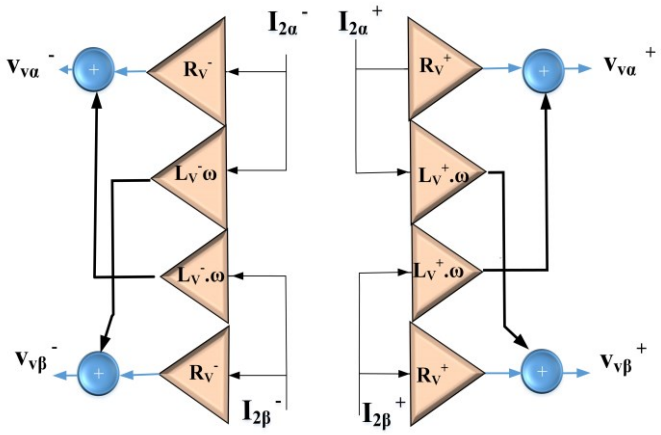


Fig. 2-Negative sequence capacitive-resistive and positive sequence inductive-resistive virtual impedance

(jwL_V^-).The capacitive virtual impedance compensates the effect of line inductance; therefore power quality can be enhanced.

In this paper, the described virtual impedance is added for compensation of PCC voltage to the parallel current and voltage controller based method.

Virtual admittance is also proposed for power quality compensating. The DG units act as designed admittance which is parallel with the local load at selected frequency. Like virtual impedance, for implementation of negative virtual admittance, firstly, the negative sequence of voltage should be extracted. After that, the desired amount of the virtual admittance will be applied to the inverter. In this paper, conductive virtual admittance is used. Using it, the inverter acts like a parallel resistance with unbalanced load and it can create a path for negative sequence current. The virtual admittance is generated by following equation:

$$\begin{bmatrix} I_{ref,N\alpha} \\ I_{ref,N\beta} \end{bmatrix} = G^- \begin{bmatrix} V_{o,\alpha}^- \\ V_{o,\beta}^- \end{bmatrix} = G^- \left[\frac{2\omega_E s}{S^2 + 2\omega_E s + (2\pi f)^2}\right] \left[T_{\alpha\beta}\right]^{-1} \begin{bmatrix} V_{o\alpha} \\ V_{o\beta} \end{bmatrix} \quad (4)$$

where G^- is virtual conductance at negative sequence frequency. $I_{ref,N\alpha}$ and $I_{ref,N\beta}$ are the reference values for current controller in this mode. The behavior of the virtual admittance is shown in Fig. 3.

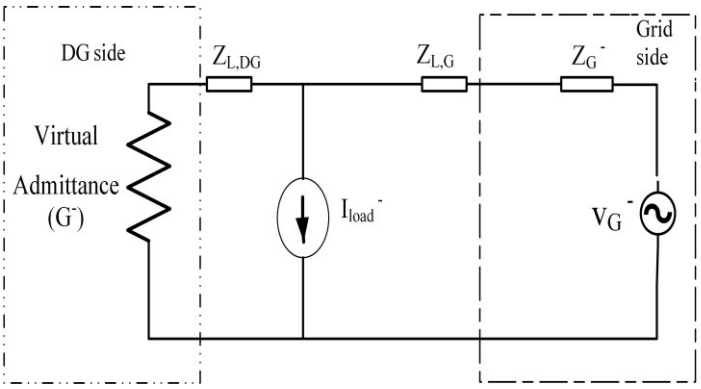


Fig. 3- The performance of Virtual admittance in negative sequence

In this figure, $Z_{L,DG}$ and $Z_{L,G}$ represent the distribution line impedance of the DG and grid. Z_G^- and V_G^- represent the negative sequence impedance and voltage of the grid.

III. SIMULATION RESULTS

The proposed control system is used for a grid connected DG unit which is shown in Fig.4. As shown in this figure, a load is also supplied by DG and grid at PCC. Since the negative sequence voltage passes through the line and the grid side of the LCL filter, the voltage unbalance occurs at PCC. The parameters of control and power systems are listed in TABLE I. It should be mentioned that the grid voltage is also assumed to be unbalanced with VUF=2.25%.

For evaluation of the voltage unbalance compensation, voltage unbalance factor (VUF) which is expressed by the following

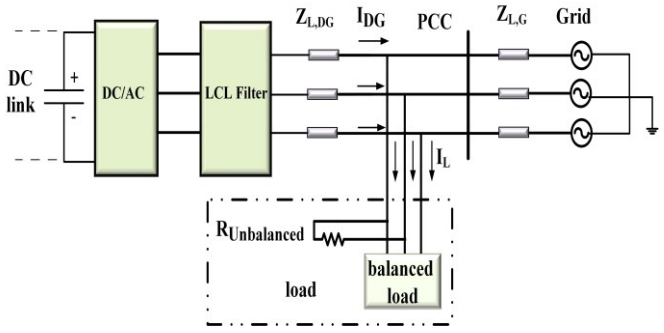


Fig.4- The grid connected system with unbalanced load

TABLE I

THE PARAMETERS OF SIMULATED SYSTEM

Parameter of DG unit	Value
L1, R1	2 mH and 0. 5 Ω
L2, R2	0.5 mH and 0.5 Ω
$Z_{L,G}$ /$Z_{L,DG}$	3mH and 0.8 Ω /1.5mH and .5Ω
Filter capacitor and damping resistance of capacitor	25 uF and 0.75 Ω
DC link Voltage	650 V
Nominal RMS line-line Voltage and frequency	400V and 50 Hz
Rated active power Rated reactive power	16 kW 6 kW
Switching frequency	10 kHz
M_P and M_I	1×10^{-5} and 1×10^{-4}
N_P and N_I	0.05 and 0.1
Cutoff frequency of low pass filter	3 rad/s
Controller parameter	Value
K_v	500
K_{II}	400
K_D	18
ω_E	62.8 rad/s
ω_b	3 rad/s
G^-	10
Positive sequence virtual impedance (R_v^+ and L_V^+)	1 Ω and 2 mH
Negative sequence virtual impedance (R_v^+ and L_V^-)	0.01, -2 mH

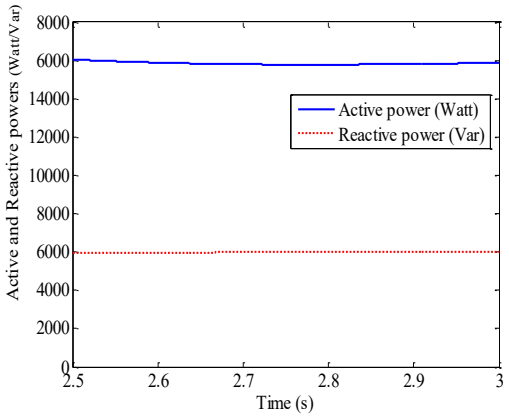
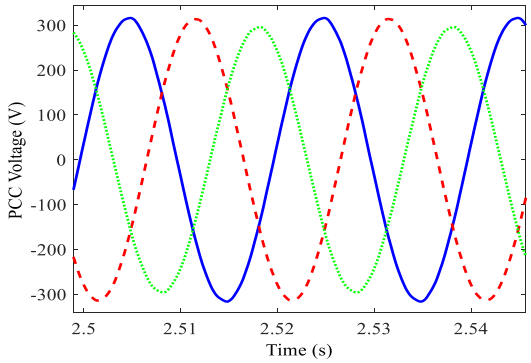


Fig.5- Active and reactive power

equation is utilized:

$$VUF = \frac{V_{rms}^-}{V_{rms}^+} \times 100 \qquad (5)$$

At the first step, the voltage unbalance compensation of the PCC is inactive. The steady state active and reactive powers which are injected by inverter are shown in Fig.5. As shown in this figure, the controller can track the reference active and reactive powers.



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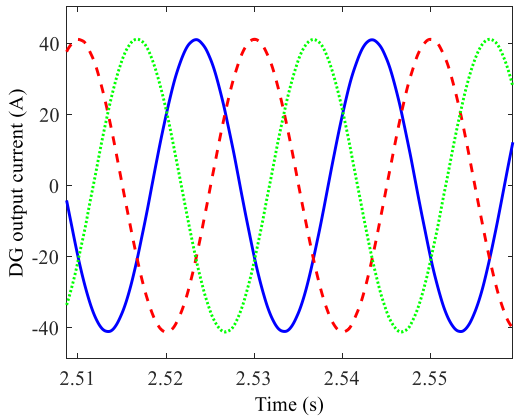
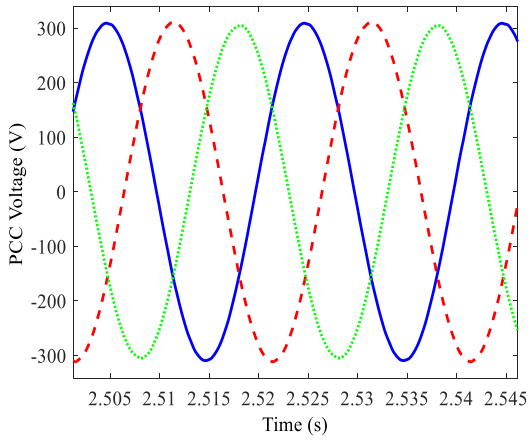


b)

Fig. 6- Three phase waveforms without any compensation, a) PCC voltage (VUF=4.2. %), b) DG current



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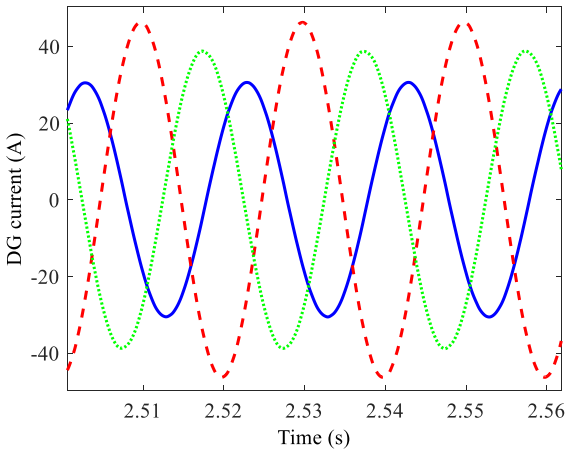


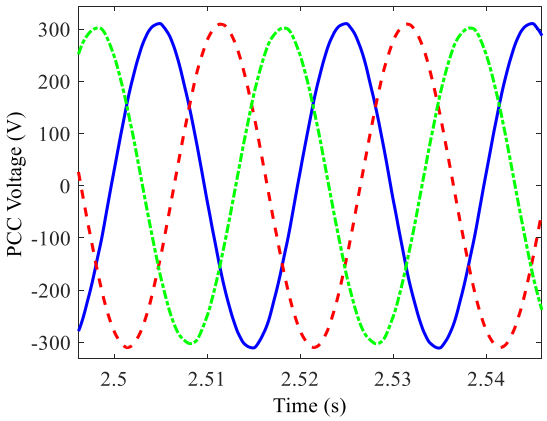
b)

Fig. 7- Three phase waveforms with negative sequence virtual impedance, a) PCC voltage (VUF=2.12%), b) DG current

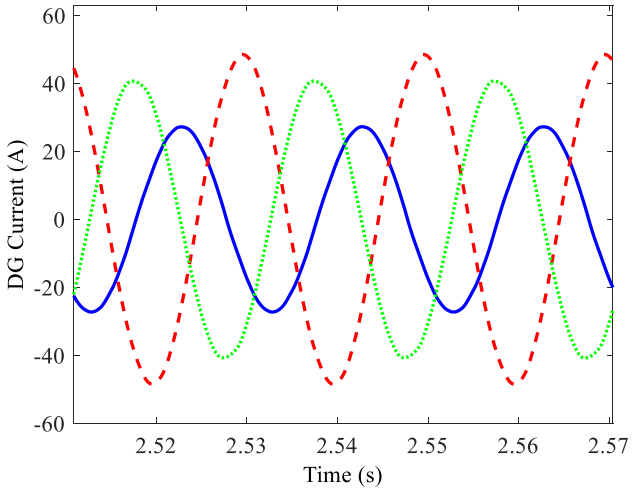
The PCC voltage is depicted in Fig.6.a. The VUF of the voltage is measured 4.2% which exceeds the standard VUF=2%, so the voltage compensation is required. It should be mentioned that the reference value of current controller is set to zero ($I_{2\alpha\beta,ref}$=0), so the DG acts as conventional inverter without any voltage unbalance compensation. The current of DG unit in this mode is depicted in Fig.6.b which shows that the DG current is balanced.

At the second simulation, the virtual impedance is activated The amount of negative sequence capacitive virtual impedance is set at L=-2 mH for compensating the grid side filter and $Z_{L,DG}$. The PCC voltage waveform is shown in Fig.7.a. The measured VUF is 2.12 % which shows that the PCC voltage compensation is achieved. The waveform of the current is also demonstrated in Fig.7.b. It shows that the DG unit injects negative sequence current to compensate the PCC unbalance voltage.

In the last scenario, the virtual admittance is activated. In this mode, the $i_{2\alpha\beta,ref}$ is selected as the $V_{o\alpha\beta}$ $\bar{G}$ according to Equ.4.



a)



b)

Fig. 8- Three phase waveforms with negative sequence virtual admittance, a) PCC voltage (VUF=0. 5%), b) DG current

The PCC voltage when using the virtual conductance is depicted in Fig.8.a with VUF=0. 5%. As shown in this figure, the voltage unbalance compensation of the load is obtained and the VUF of is under 2%. This is achieved as the result of creating a low impedance current path for unbalance current from the DG. The current of the DG is also depicted in Fig. 8.b.

The simulation results show that the PCC voltage unbalance compensation can be achieved by both of negative sequence virtual admittance and impedance method. The voltage unbalance compensation, using virtual impedance needs the knowledge about the line impedance. Although, the inductance of the DG line and grid side filter is fully compensated by capacitive virtual impedance, the VUF of voltage is above the 2%. Using the negative sequence virtual admittance, the voltage unbalance can be effectively compensated, since it can create a low impedance path for the current.

IV. CONCLUSION

In this paper, voltage unbalance compensation of PCC voltage is proposed. This compensation is implemented using virtual impedance and admittance in stationary frame with parallel voltage and current controllers. The simulation results show that using both methods, the voltage unbalance will be compensated. Using the negative sequence capacitive virtual impedance can compensate the negative sequence droop across the grid side filter (L_2) of interfacing inverter and the DG transmission line and it can enhance the power quality of the PCC; However, it needs the knowledge of the line impedance and the VUF of PCC voltage is above 2%.

In other hand, using virtual admittance can create a low impedance path for unbalance current from the DG and the DG unit acts as a parallel conductance with the unbalance load. In other word, using virtual admittance, the unbalance load is compensated locally by DG and the power quality will be enhanced; Furthermore, the VUF of the PCC voltage is measured below of the standard limit of 2% by using virtual admittance approach. It shows that by using the virtual admittance, the PCC voltage unbalance compensation is more effective than using virtual impedance in this grid connected MG.

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