A Power Quality Improved Bridgeless Converter Based Computer Power Supply

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Abstract— **Poor power quality, slow dynamic response, reduced output voltage regulation, high device stress, harmonic rich, periodically dense, peaky, distorted input current are the major problems which are frequently encountered in conventional switched mode power supplies (SMPSs) used in computers. To mitigate these problems, it is proposed here to use a non-isolated bridgeless buck-boost single ended primary inductance converter (SEPIC) in discontinuous conduction mode (DCM) at the front end of an SMPS. The bridgeless SEPIC at the front end provides stiffly regulated output dc voltage even under frequent input voltage variations and loads. The output of the front end converter is connected to a half bridge dc-dc converter for isolation and also for obtaining different dc voltage levels at the output that are needed in a computer. Controlling a single output voltage is able to regulate all the other dc output voltages as well. The design and simulation of the proposed power supply is carried out for obtaining improved power quality which is verified through the experimental results.**

Keywords— Bridgeless converter; PFC; input current; computer power supply

I. INTRODUCTION

Many electronic appliances powered up from the utility utilize the classical method of ac-dc rectification which involves a diode bridge rectifier (DBR) followed by a large electrolytic capacitor. The uncontrolled charging and discharging of this capacitor instigates a harmonic rich current being drawn from the utility which goes against the international power quality standard limits [1-2]. Modern ac-dc converters incorporate power factor correction (PFC) and harmonic current reduction at the point of common coupling (PCC) which improves voltage regulation and efficiency [3-5] at the load end. Personal computer is one of the electronic equipment which is severely affected by power quality problems. Single stage and two stage conversion of ac voltage into dc voltage have been used in computers to maintain harmonic content within limits and also to obtain stiffly regulated multiple outputs. Single stage power conversion is simple, compact and cost-effective. However, it suffers from poor dynamic response, control complexity, high capacitance value and high component stress. So, two stage conversion of ac voltage into multiple dc voltages is mostly preferred in computers [6]. The component count of the two stage power supply is high in comparison to its single stage counterpart; also, it provides better output voltage regulation, fast dynamic response and blocks the 100Hz component in the first stage itself so that large capacitors at the output side are avoided.

Various front end converters have been employed in the power supplies for providing PFC and output voltage regulation. A boost converter is the common choice for providing PFC in power supplies. However, it is not the preferred choice in computer power supplies due to its large input voltage range [7]. The output voltage of a boost converter cannot be controlled to a value less than 300V for a 220V ac input supply. Therefore, buck-boost converter is preferred in computers where wide variations in input voltages and load are expected [8-9]. The efficiency of a two stage SMPS is lower than the conventional SMPS; to eliminate this disadvantage, a new bridgeless front end converter is proposed in this paper for computer power supplies. The elimination of DBR at the front end results in reduced conduction losses and large output voltage range with enhanced efficiency [10-13]. At the output of the front end converter, a half bridge converter is used which provides isolation, regulation and multiple dc outputs [14-16]. The half bridge converter is a common choice because it offers better core utilization.

It is observed from the available literature that the power quality improvement in SMPSs using bridgeless PFC converter has not been attempted by many researchers so far. In this work, a bridgeless single ended primary inductance converter (SEPIC) is used at the front end of the SMPS. Test results of the proposed multiple-output SMPS are found in line with the simulated performance demonstrating its improved power quality and output voltage regulation.

II. SMPS CONFIGURATION AND OPERATING PRINCIPLE

The proposed computer power supply consists of mainly two parts, bridgeless front end ac-dc converter and multi-output isolated dc-dc converter. The front end converter is designed in discontinuous conduction mode (DCM) for achieving inherent PFC while the isolated converter is designed in continuous conduction mode (CCM). The control loops of both converters are independent of each other. The system configuration and operating principle of the SMPS system has been described in the following subsections.

A. System Configuration

The configuration of proposed power supply with four regulated dc output voltages is shown in Fig.1. At the input side, DBR is eliminated by using two SEPICs. The upper converter operates in the positive half cycle and the lower one in the negative half cycle of the input ac voltage. The switching frequency of both the converters is set at 20kHz for efficient control. The design of output inductors for both the converters is carried out in DCM to reduce the complexity in control. The regulation of the output voltage is able to take care of wide variations in the input voltage and load. The output dc voltage is sensed and compared with a reference voltage from which the voltage error is obtained which is given to a proportional and integral (PI) controller; the PI controller output is compared with a high frequency saw-tooth wave to yield PWM pulses that are given to both switches simultaneously. The width of these PWM pulses varies

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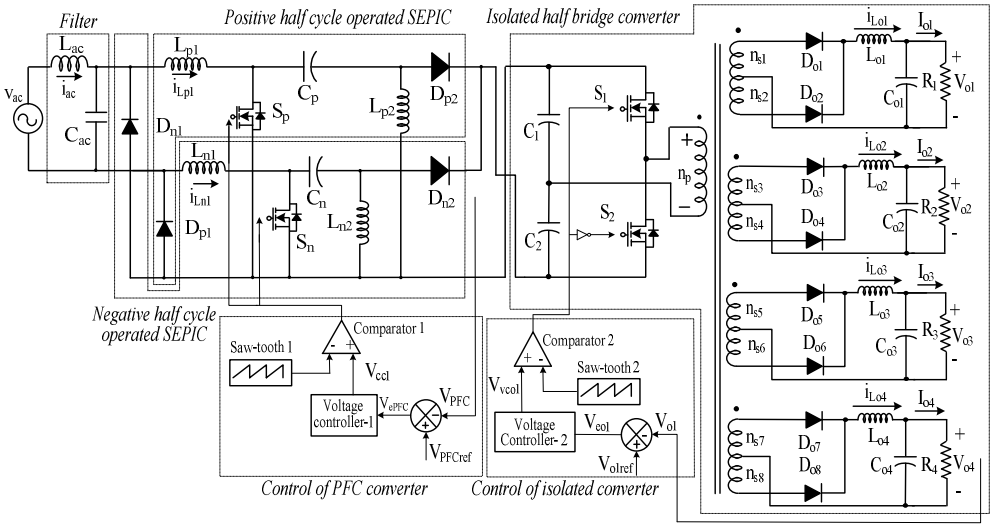


Fig.1 Schematic diagram of PFC converter based SMPS

according to the output of the PI controller so that the output dc voltage is regulated effectively which is, in turn, fed to the isolated half bridge converter in the second stage to obtain multiple isolated regulated output voltages. The isolation is effected through multi-winding high frequency transformer (HFT). A centre tapped configuration is chosen at the output side to reduce the conduction losses. All the secondary windings are controlled via one control loop. The highest rated secondary winding of the HFT is selected for voltage sensing. The difference between the output voltage and reference voltage is fed to another PI controller whose output is compared with another high frequency saw-tooth wave to generate second set of PWM signals for the half-bridge converter devices S_1 and S_2. Care should be taken to make sure that there is sufficient dead-time between turning OFF of S_1 and turn-ON of S_2 to avoid shoot-through. The isolated converter is operated in CCM to take the advantage of reduced stress. If the load in any of the winding changes, the duty cycle changes accordingly to ensure regulated dc outputs. The response of the other outputs is slower than the one where the output voltage is sensed.

B. Operating Principle

T operation of the front end converters and the isolated converter are described independently as follows:

1) Operating principle of the front end converter

During the positive half cycle of the input voltage, the upper SEPIC operates as shown in Fig. 2. In the same way, during negative half cycle the lower SEPIC would operate. The operation of the SEPIC in one PWM cycle is described with the help of the following modes: In the first mode, the high frequency switch S_p turns on, the input inductor L_{p1} starts storing the energy which is transferred from the single phase ac mains as shown in Fig. 3a. Diode D_{p1} completes the current path. In the second mode, S_p is turned off and diode D_{p2} starts conducting. The energy in output inductor L_{p2} starts decreasing to zero which is shown in Fig. 3b. In the last switching state, the current in the output inductor remains zero until the start of next switching cycle. This mode ensures the DCM operation as shown in Fig. 3c.

2) Operating principle of isolated converter

Two high frequency switches are turned on and off alternately in one switching cycle. So, the operation of the converter in one half of the switching cycle is the same as that

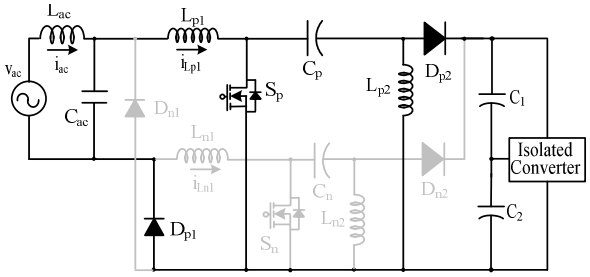


Fig. 2 Operation of PFC converter when the input voltage is positive

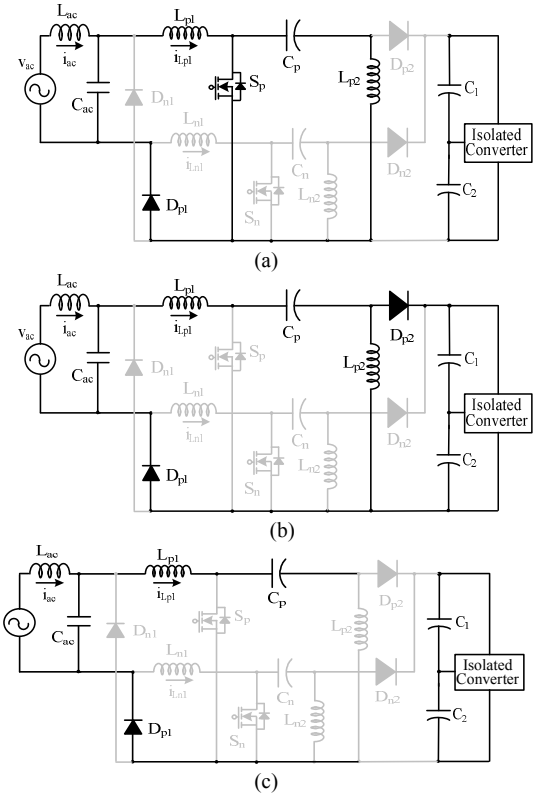


Fig. 3 Operating modes of bridgeless PFC converter when the input voltage is positive

of the other half cycle. In the first half cycle, the upper switch S_1 is turned on. The diodes on the secondary side start conducting and the inductors in all the secondary windings start storing energy. All the filter capacitors discharge through the loads to maintain dc output voltages as constants. In the

next half cycle of the PWM period, the upper switch is turned off. The secondary diodes are turned on to free-wheel the inductors currents. The current in the all the secondary windings cancel the core flux so that the net voltage across the HFT becomes zero.

III. Design of the Proposed Bridgeless Converter Based SMPS System

The design of the proposed bridgeless converter based SMPS is described in the following section.

A. Design of PFC Bridgeless Converter Based SMPS System

The design for the positive half cycle operated PFC converter is carried out here. The negative half cycle operated converter is designed in the same way. The average voltage V_{acav} is calculated as,

$$V_{acav}=\frac{2\sqrt{2}V_{ac}}{\pi}=\frac{2\sqrt{2}*220V}{3.14}=198V \quad (1)$$

The duty cycle D of the PFC buck-boost converter is expressed as the ratio of its output dc voltage to the sum of output dc voltage and input voltage.

$$D=\frac{V_{PFC}}{V_{PFC}+V_{acav}}=\frac{300V}{300V+198V}=0.6 \quad (2)$$

Irrespective of variation in the input voltage from 170V to 270V, the output voltage is maintained constant at 300V. Hence, the duty cycles for supply voltages of 170V voltage, 220V and 270V are calculated as, D_{170V}=0.66, D_{220V}=0.6, D_{270V}=0.552 respectively. The duty cycle D of the PFC converter is taken less than D_{220V} for an efficient control during DCM operation. Therefore, it is considered as 0.25 for the design of the PFC converter.

The input inductor value is calculated for the permitted ripple of 40% of input current.

$$L_{p1}=\frac{DV_{acavg}}{f*(i_{in\,ripple})}=\frac{0.25*198V}{20kHz*0.58A}=4.35mH \quad (3)$$

where, f is the switching frequency of the PFC converter.

The critical conduction parameter is given as,

$$K_a<\frac{1}{2(\frac{V_{PFC}}{\sqrt{2}V_{ac}}+n)^2}=\frac{1}{2(\frac{300V}{311V}+1)^2}=0.129 \quad (4)$$

where, n is taken as 1 for the non-isolated PFC converter. To operate the PFC converter in DCM, the conduction parameter should be taken less than K_a for efficient control. Hence, it is selected as 0.08.

The equivalent value of inductance of the PFC converter is given as,

$$L_{eq}=\frac{R_{dc}K_a}{2f}=\frac{281.2\Omega*0.08}{2*20kHz}=225\mu H \quad (5)$$

Therefore, the output inductor value is calculated as,

$$L_{p2}=\frac{L_{p1}L_{eq}}{L_{p1}-L_{eq}}=\frac{4.31mH*225\mu H}{4.31mH-225\mu H}=225\mu H \quad (6)$$

Therefore, the 100µH is selected to ensure DCM condition and unity PF operation at a low input voltage.

The intermediate capacitor value is estimated as,

$$C_p=\frac{1}{\omega_r^2(L_{p1}+L_{p2})}=\frac{1}{2*\pi*2000Hz(4.3mH+0.1mH)}=0.18\mu F \quad (7)$$

where, ω_r is the angular frequency ($\omega_r=2\pi f_r$). A f_r is considered as 2000Hz ($f>f_r>f_L$).A capacitor value of 0.22µF is selected for the hardware implementation.

An L-C filer is used at the input side to mitigate higher order harmonics [18]. The maximum value of capacitor is,

$$C_m=\frac{I_p\tan\theta}{\omega V_p}=\frac{2.25A*0.017}{314*311V}=391nF \quad (8)$$

The filter capacitor value is selected such that it is less than C_m. Hence, a 330nF capacitor is selected in hardware implementation.

The filter inductor L_d is calculated for mitigating higher order harmonics.

$$L_d=\frac{1}{4*\pi^2*f_c^2*C_d}=\frac{1}{4*(3.14*5*10^3)^2*330*10^{-9}}=3.07mH \quad (9)$$

A 3.1mH of inductor is selected for simulation and experimental system.

The input capacitors of the isolated half bridge dc-dc converter act as the output filter capacitors for the PFC converter. So, the design of the capacitor is very important to eliminate the second order harmonic component as well as to provide maximum power for that duration when input voltage falls. This is very crucial for PC power supplies as the rating of the capacitor affects the size and the cost of the overall SMPS.

The expression for calculating the capacitor to reduce second order harmonic is [3],

$$\frac{C_1}{2}=\frac{C_2}{2}=\frac{I_{PFC}}{2\omega\Delta V_{PFC}}=\frac{1.06A}{2*314*6V}=0.28mF \quad (10)$$

The hold-up capability can be estimated as,

$$t_{hold\text{-}up}=(V_{PFCm}^2-V_{PFCmin}^2)\frac{C}{2*P_o} \quad (11)$$

where, $t_{hold\text{-}up}$ is the holdup time of the capacitor, P_o is the maximum output power, V_{PFCm} is the minimum output voltage (2% ripple is considered) and V_{PFCmin} is the minimum voltage at which the output voltage holds regulation.

Therefore, to maintain 10ms hold-up time, the required capacitance is calculated as,

$$C=\frac{t_{hold\text{-}up}*2*P_o}{(V_{PFCm}^2-V_{PFCmin}^2)}=\frac{10ms*2*320W}{(294V)^2-(260V)^2}=0.339mF \quad (12)$$

Two capacitors are connected in series. Therefore, the value of C_1=C_2=0.679mF. The selected value of the capacitors is 0.6mF each to meet both the conditions.

The calculation of inductance for the secondary winding with highest rating is shown here, while the calculation for rest of the secondary windings remains same. The inductance L_{o1} is expressed as,

$$L_{o1}=\frac{V_{o1}(0.5-D_s)}{\Delta i_{Lo1}*f_s}=\frac{12V(0.5-0.4)}{0.625A*60kHz}=0.032mH \quad (13)$$

Similarly, the inductances for the other secondary windings are calculated as 9.5 µH, 6.8 µH and 1.5mH.

IV. Simulated Performance of Power Supply

The performance of proposed power supply is simulated to obtain its performance indices such as input voltage/current, input inductors(L_{p1}, L_{n1}), output inductors (L_{p2}, L_{n2}), intermediate capacitor (C_p, C_n), output voltage (V_{PFC}) and output voltages/current (V_{o1}/I_{o1}, V_{o2}/I_{o2}, V_{o3}/I_{o3}, V_{o4}/I_{o4}). The simulated performance is discussed in the following sections.

A. Full Load Performance

Full load performance of the PFC bridgeless converter based computer SMPS is shown in Fig. 4. The input ac voltage and current are found to be sinusoidal with a harmonic distortion of 3.33% as shown in Figs. 4a and 4b. The output voltages are maintained constant with their respective output

currents. The waveforms at various test points of the bridgeless PFC converters are shown in Fig. 4c. The currents of input inductors of both the converters are shown which are maintained in CCM. The voltage across the intermediate capacitor is observed of the order of 450V which is quite satisfactory. The waveform of currents of output inductor of both positive half cycle and negative half cycle operated PFC converter demonstrates the DCM operation and the peak current in both the converters is observed to be about 17A. Both the converters operate in positive and negative half cycles of input voltage alternately. This validates the bridgeless operation of the power supply. The peak voltage stress and current stress across the switch is observed of the order of 520V and 17A which are within acceptable limits.

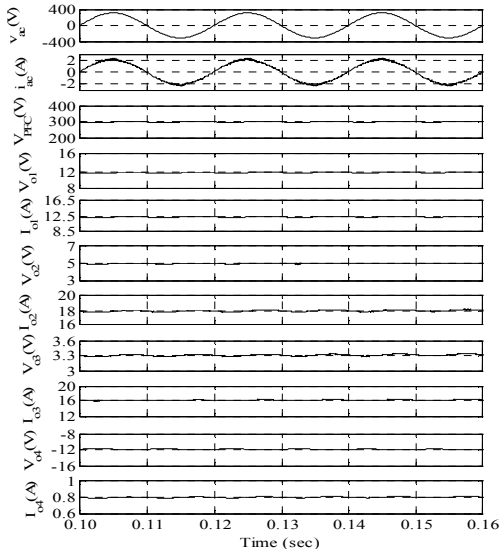


Fig.4a Performance of the computer power supply at rated condition

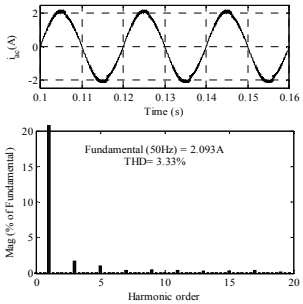


Fig. 4b Input current and its harmonic spectrum at full load condition

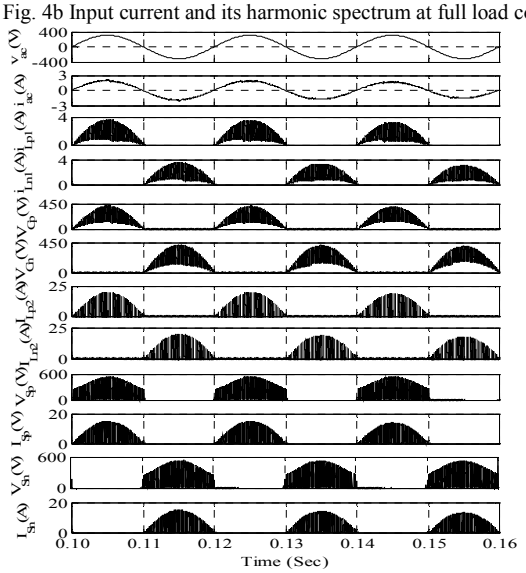


Fig. 4c Waveform of various components of bridgeless converter

B. Light Load Performance

Light load performance of the power supply is shown in Fig. 5a and 5b. Loads on +12V and +5V outputs are reduced simultaneously at 0.15s to demonstrate its dynamic performance. The output current is reduced from 12.5A to 3.75A and 18A to 9A as the load is perturbed. The input current is maintained sinusoidal and co-phase with input voltage. The input current THD at the light load condition is observed of the order of 3.76% as shown in Fig. 5b.

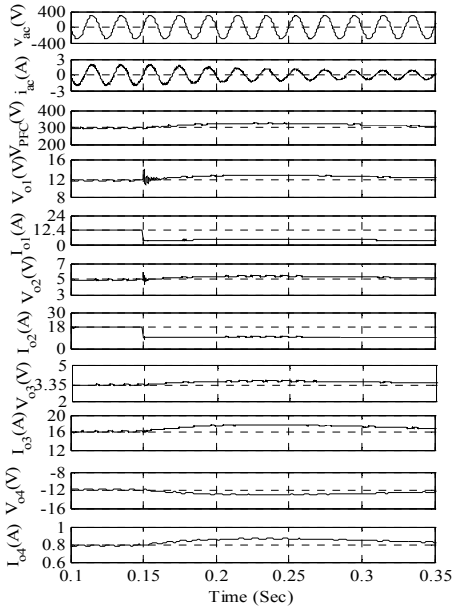


Fig.5a Performance of the computer power supply at light load condition

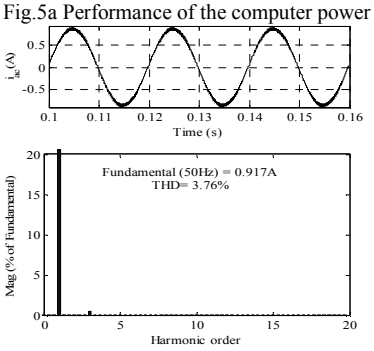


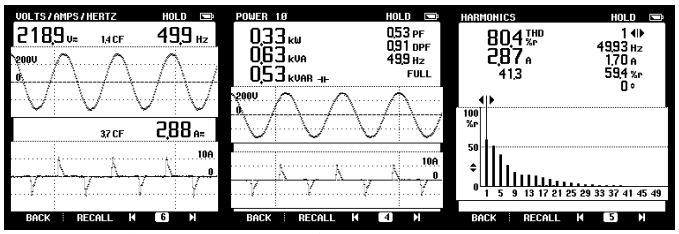
Fig. 5b Input current and its harmonic spectrum at light load condition

V. EXPERIMENTAL PERFORMANCE OF PROPOSED BRIDGELESS CONVERTER BASED SMPS

The hardware prototype of the bridgeless PFC converter based computer SMPS is developed to validate the simulated performance. For close loop control, a digital signal processor (DSP) TI-TMS320F2812 is used which provides the PWM pulses to both the switches simultaneously by using PWM channels. The recorded performance of the power supply is described as follows.

A. Performance of Conventional SMPS

The conventional computer SMPS draws a harmonic rich, distorted peaky input current with a high crest factor and low PF form the single phase ac mains. The THD of the input current is observed of the order of 80% and the PF is 0.4 which affects the distribution system as shown in Fig. 6. This violates the set guidelines of harmonic emission and is not recommended by the power quality standards. Therefore, it is highly recommended to improve the power quality of the conventional computer SMPS.



(a) (b) (c)

Fig. 6 (a) Recorded waveform of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at light load condition

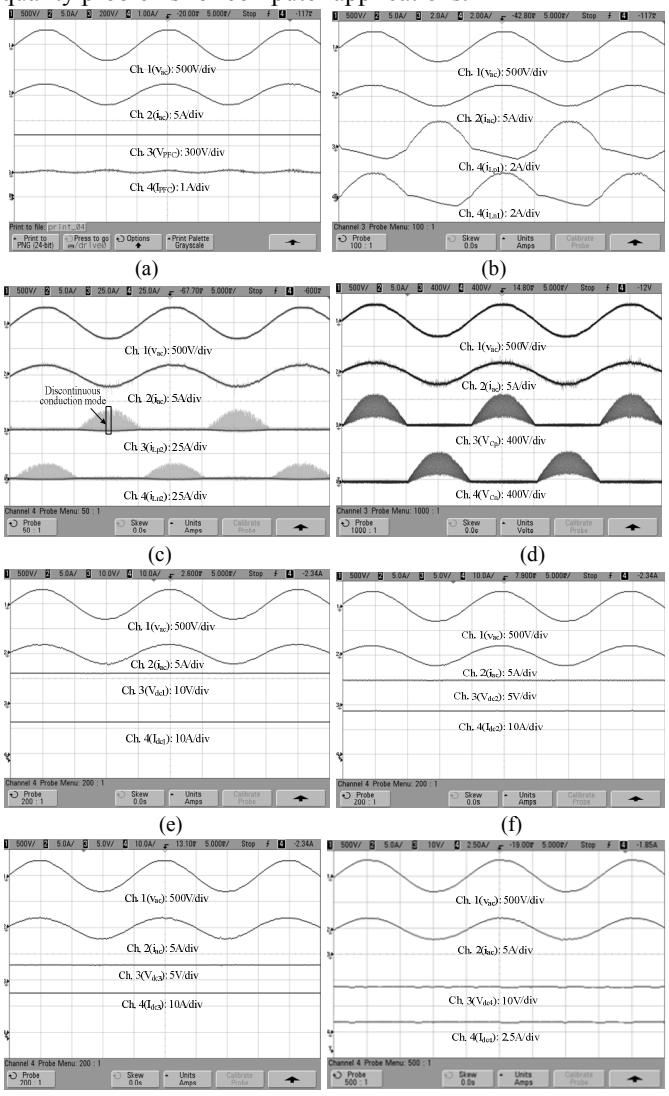
B. Performance of SMPS under Varying Input Voltages

The performance of the PFC bridgeless converter based SMPS is shown in Fig.7 which is recorded at full load and rated voltage condition. Fig. 7a is the recorded waveform of input and output voltage and current. The unity PF operation is obtained with the input current being sinusoidal while the output voltage of the PFC converter is regulated to 300V. The inductor current of positive half cycle converter i_{Lp1} and the negative half cycle operated converter i_{Ln1} are shown in Fig. 7b and are in CCM as per the design. The inductor current of positive half cycle converter i_{Lp1} operates in positive half cycle of the input voltage and inductor current of negative half cycle converter L_{n1} operates when the input voltage is negative. Fig. 7c shows the recorded waveforms of output inductor currents i_{Lp2} and $i_{Ln2}$of positive and negative half cycle converters. Both the currents touch zero in each switching cycle which verifies the design criteria of inductor being in DCM. The upper inductor operates in DCM when input voltage is positive and the lower inductor operates in DCM when the input voltage is negative. The capacitor voltages of both the converters are shown in Fig. 7d which operates alternately in positive and negative half cycles of input voltage and are in CCM as per the design. The recorded waveforms of regulated dc output voltages +12V, +5V, +3.3V and -12V with their respective currents are shown in Fig. 7(e)-(h). The recorded full load performance of PFC converter based SMPS is shown in Fig. 8. The input current THD in this condition is recorded as 6.5%. To demonstrate the performance of SMPS at wide input voltage range, the test results are recorded at 170V and 270V condition and are presented in Figs. 9 and 10. At 170V-270V, the input current remains sinusoidal while the PF is maintained to unity. The dynamic performance during input voltage variation is shown in Fig. 11. The output voltage is maintained constant within few power cycles of input voltage.

C. Performance of SMPS Under Light Load

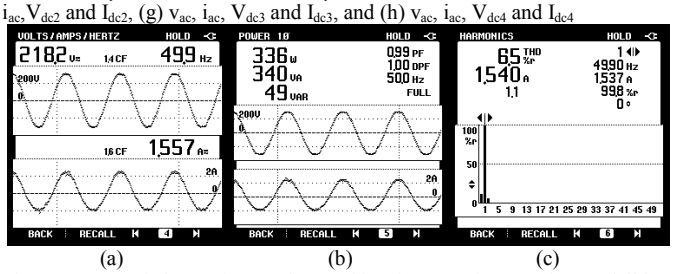
The light load performance of SMPS is recorded by switching on and off some loads and is shown in Fig. 12. The recorded test results demonstrate the fairly improved power quality and the input current being sinusoidal with its THD being 7.3% which is within the limit set by IEC 6100-3-2. Fig. 13 shows the recoded waveform of input and output voltages and currents when a step change is applied in load. The output voltage remains constant while the input current is changed to maintain the power balance.

The component count of the proposed bridgeless PFC converter based power supply is high because two PFC converters are added in the front end in comparison to the classical PFC based SMPS. However, the input current in the proposed SMPS flows through fewer components compared to the classical PFC based power supply. Therefore, the efficiency of the bridgeless PFC converter based SMPS is higher than the conventional PFC converter based SMPS. Table I shows the comparison of PFC based SMPS and proposed SMPS system. Test results demonstrate the excellent performance of the proposed bridgeless converter based SMPS under all operating conditions and hence it can be recommended as an effective solution for mitigation of power quality problems for computer applications.



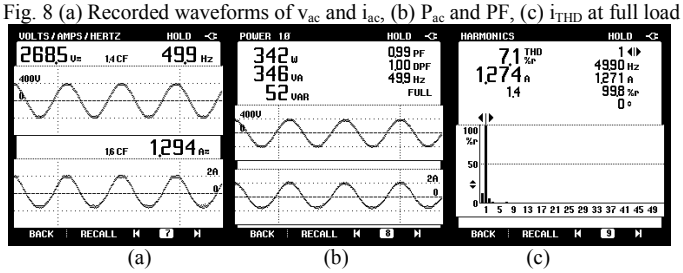
(a) (b) (c) (d) (e) (f) (g) (h)

Fig. 7 Recorded waveforms of (a) v_{ac}, i_{ac}, V_{PFC} and I_{PFC}, (b) v_{ac}, i_{ac}, i_{Lp1} and i_{Ln1}, (c) v_{ac}, i_{ac}, i_{Lp2} and i_{Ln2}, (d) v_{ac}, i_{ac}, V_{Cp} and V_{Cn}, (e) v_{ac}, i_{ac}, V_{dc1} and I_{dc1}, (f) v_{ac}, i_{ac},V_{dc2} and I_{dc2}, (g) v_{ac}, i_{ac}, V_{dc3} and I_{dc3}, and (h) v_{ac}, i_{ac}, V_{dc4} and I_{dc4}



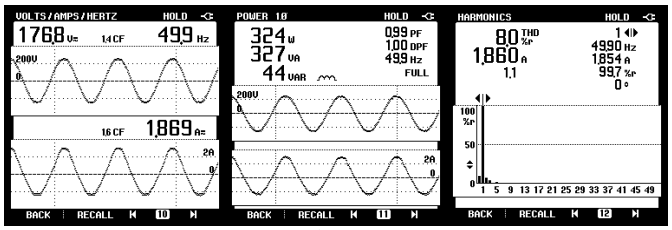
(a) (b) (c)

Fig. 8 (a) Recorded waveforms of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at full load



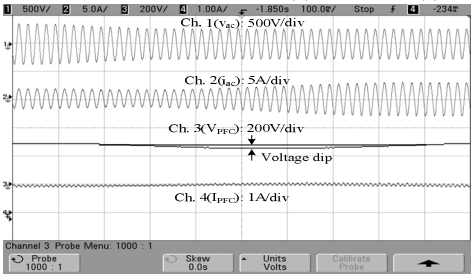
(a) (b) (c)

Fig. 9 (a) Recorded waveforms of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at 270V



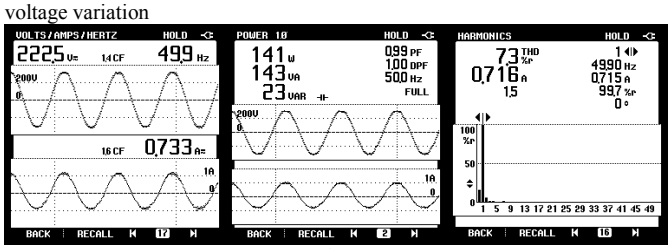
(a) (b) (c)

Fig. 10 (a) Recorded waveforms of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at 170V



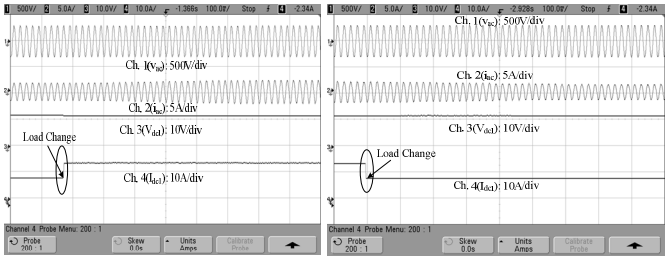
(a)

Fig. 11 (a) Recorded waveforms of v_{ac}, i_{ac}, V_{PFC} and I_{PFC} during ac input voltage variation



(a) (b) (c)

Fig. 12 (a) Recorded waveform of v_{ac} and i_{ac}, (b) P_{ac} and PF, (c) i_{THD} at light load condition



(a) (b)

Fig. 13 (a) Recorded waveform of load increase in I_{dc1} (b) Recorded waveform of load decrease in I_{dc1}

TABLE-I
COMPARISON BETWEEN CLASSICAL PFC AND PROPOSED PFC

Component		Conventional PFC	Proposed PFC
Slow Diode		4	2
Fast recovery diode		1	2
High frequency Switch		1	2
Current conduction path	L_{p1} charging	2 slow diodes, 1 switch	1 slow diodes, 1 switch
	L_{p1} discharging	2 slow diodes, 1 fast recovery diode	1 slow diode, 1 fast recovery diode
	L_{p1} zero current	2 slow diodes	1 slow diode

VI. CONCLUSION

A bridgeless non-isolated SEPIC based power supply has been proposed here to mitigate the power quality problems prevalent in any conventional computer power supply. The proposed power supply is able to operate satisfactorily under wide variations in input voltages and loads. The design and simulation of the proposed power supply is initially carried to demonstrate its improved performance. Further, a laboratory prototype is built and experiments are conducted on this prototype. Test results obtained are found to be in line with the simulated performance. They corroborate the fact that the power quality problems at the front end are mitigated and hence, the proposed circuit can be a recommended solution for computers and other similar appliances.

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