Bridgeless SEPIC PFC Converter for Low Total Harmonic Distortion and High Power Factor

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Abstract— **There is a need to improve the power quality of the grid as well as the power factor implied on the grid due to the nonlinear loads connected to it. A new single phase bridgeless AC/DC power factor correction (PFC) topology to improve the power factor as well as the total harmonic distortion (THD) of the utility grid is proposed in this research. By eliminating the input bridge in conventional PFC converters, the control circuit is simplified; the total harmonics distortion THD and power factor PF are improved. The controller operates in multi loop fashion as the outer control loop calculates the reference current through innovative filtering and signal processing. Inner current loop generates PWM switching signals through the PI controller. Analytical derivation of the proposed converter is presented in detail. Performance of the proposed PFC topology is verified for prototype using PSIM circuit simulations. The experimental system is developed, and the experimental results agree with simulation results.**

Keywords— *DSP; Bridgeless converter; power factor correction (PFC); Sepic converter; Total Harmonic Distortion THD*

I. INTRODUCTION

The request for developing power quality of the AC system has drawn excessive interest during the recent years. The increased usage of power electronic devices, such as variable speed drives, uncontrolled rectifiers and other switching devices, affects the power quality of the utility grid significantly. Standards similar to International Electro technical Commission (IEC) 61000-3-2 restrict the harmonics generated by these equipments [1]. To reduce harmonics in energy transmission lines, the research on active power factor correction (PFC) techniques has taken on an accelerated path [2-5].

Typical PFC converter topologies are boost [6,7], buck-boost [8], buck [9-11] and SEPIC [12-17]. The boost PFC converter is often used in practical applications, as the input current can be conveniently formed into a sinusoidal waveform to obtain unity power factor. However, the boost PFC converter has a restricted capability since the DC output voltage must be higher than the peak value of the AC input voltage [8]. On the other hand, the DC output voltage of the buck PFC is lower than the peak of the AC input voltage, which allows reducing components ratings and the cost. [11]. A buck PFC converter procures an alternative for low-voltage applications such as a 48V DC bus. Moreover, the buck PFC

can obtain high efficiency over the entire input voltage range with distorted input current that comfortably passes the limits imposed by IEC 61000-3-2 requirements [1].

The input current of the buck PFC converter has dead zones along the cycle, which requires extensive passive filtering to improve the power factor. There is a tradeoff between output voltage choice and power factor. To solve this problem, SEPIC or Cuk converters were proposed. A conventional SEPIC converter can supply a high power factor in wide range of voltage conditions [12-13]. The output voltage could be reduced or increased without the need of inversion with the SEPIC converters [14].

This paper presents a new topology for single phase bridgeless AC/DC PFC converters that reduces the THD and improves the PF of the operation. Proposed SEPIC converter combines the bridge and DC-DC stages into one stage. Section 2 analyses operation of the proposed SEPIC PFC converter. In Section 3, component selection and control circuit design are presented. The simulation results of the conventional and proposed SEPIC converter are presented in Section 4. Summary and future work is provided in Section 5.

II. PROPOSED BRIDGELESS SEPIC PFC CONVERTER

The conventional SEPIC PFC converter is shown in Figure 1 [15]. The operation of the circuit can be separated in to two modes concerning the position of the switches. When the switch Q_1 switched on, output diode D is reverse biased. The input inductor L_1 starts to charge, output inductor L_2 and AC input capacitor C_1 creates a resonant circuit. Here, load draws current from the output capacitor C_0. During this situation, the voltage of the input inductor will be same as the rectified AC voltage V_{ac}. Besides input capacitor's voltage and output inductor's voltage are equal to V_{ac} during this mode of operation. In the second mode, the switch is turned off, diode is forward biased and L_1, C_1, L_2 creates a loop. The load is directly connected to the inductors during this mode, which discharges them during the mode of operation.

The proposed bridgeless SEPIC PFC converter with three active switches is shown in Figure 2. When Q_1, Q_3 and Q_4 turn on, input inductor currents starts to increase linearly. The

output inductor voltage is equal to the voltage of C_1 which was equal input voltage before the switches are turned on. Thereby, i_{L2} reduces linearly. This mode finishes by turning off Q_1, Q_3 and Q_4. By turning Q_1, Q_3 and Q_4 off, D starts to conduct. Input inductor current reduces linearly and i_{L2} increases linearly until the diode current extinguishes. When D turns off, output side is disengaged from the input side, the current through the inductors freewheel at the input side. Working modes for proposed SEPIC PFC converter is provided in Figure 3.
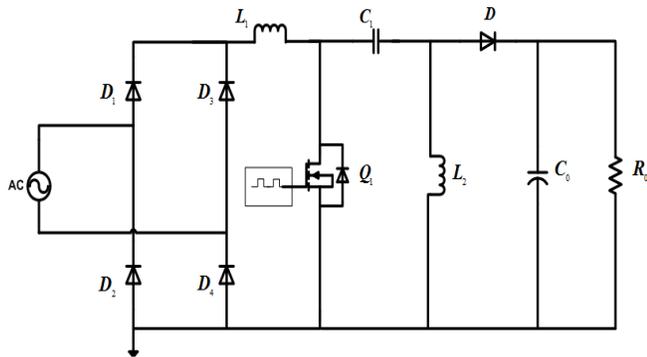
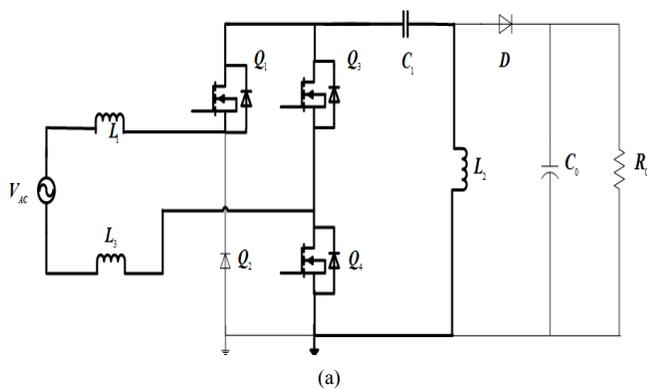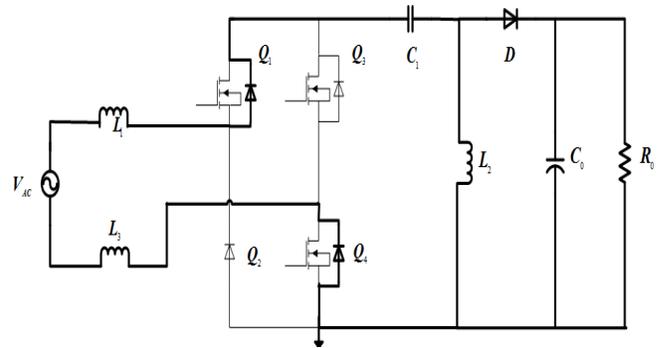

Fig. 1.   Conventional SEPIC PFC converter
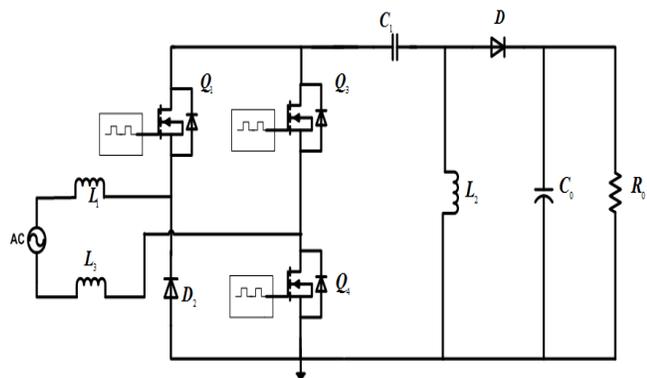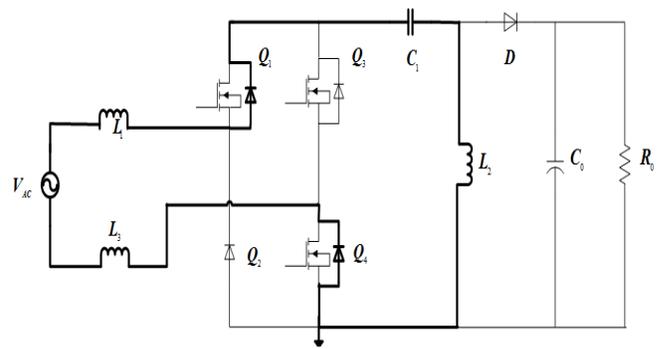

Fig. 2.   Proposed SEPIC PFC converter circuits

(a)

(b)

(c)

Fig. 3.   Each operating mode for proposed SEPIC PFC converter circuits

III.   PRINCIPLE OF OPERATION

Since the proposed SEPIC converter circuit comprises of two symmetrical structures as shown in Fig. 3, the circuit is investigated for the positive half cycle structure. Suggesting that the circuit working in a positive half cycle of a switching period T_s can be divided into three working modes, as shown in Fig. 3(a)–(c) and it can be defined as follows.

Mode 1: In this mode, Q_1, Q_3 and Q_4 switches are turned on, as shown in Fig. 3(a). In this mode, the input inductor currents increase and output inductor current decreases linearly at a rate proportional to the input voltage V_{ac}. The rate of increase of the input inductor currents and the rate of decrease of output inductor current are given by

$$\frac{di_{ac}}{dt} = \frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = \frac{V_{ac}}{L_{1,3}} \qquad (1)$$

$$\frac{di_{L2}}{dt} = -\frac{V_{ac}}{L_2} \qquad (2)$$

where $L_{1,3}$ value is given by

$$\frac{1}{L_{1,3}} = \frac{1}{L_1} + \frac{1}{L_3} \tag{3}$$

Thus, the switch current is given by

$$i_{Q3} = i_{ac} - i_{L2} = \frac{V_{ac}}{L_{1,3}} + \frac{V_{ac}}{L_2} \tag{4}$$

This mode ends when Q_1, Q_3 and Q_4 switches are turned off, starting the next mode.

Mode 2: In this mode, Q_1, Q_3 and Q_4 switches are turned off, but Q_1 and Q_4 are conducting through anti parallel body diodes. Fast diode D is turned on, providing a route for the input and output inductor currents. In this mode, the input inductor currents decrease linearly at a rate that is proportional to the output voltage V_{dc} and output inductor current increase linearly. The three inductor currents are given by

$$\frac{di_{L1}}{dt} = \frac{di_{L3}}{dt} = -\frac{V_{dc}}{L_{1,3}} \tag{5}$$

$$\frac{di_{L2}}{dt} = \frac{V_{dc}}{L_2} \tag{6}$$

This mode ends when the diode current distinguishes.

Mode 3: In this mode, all the active switches are turned off, as shown in Fig. 3(c). Q_1 and Q_4 are conducting through anti parallel body diodes. This mode ends by starting the next switching cycle. In this mode, the inductors L_1, L_2 and L_3 currents are equal. The switch voltage and diode voltage are equal input voltage V_{ac} and output voltage V_{dc} respectively. The duration of this mode is

$$\Delta_1 = \frac{V_{ac}}{V_{dc}} \times d \tag{7}$$

where, d is the duty cycle.

IV. DESIGN OF THE PROPOSED CONVERTER

The standard design equations for the main components of the AC/DC SEPIC PFC converter are provided in [15-17]. The proposed converter is designed for 25 V_{rms}, 60 Hz AC input voltage to generate at 10 V DC. The input current ripple is limited to 20% of the peak current I_{ac_peak} with the switching frequency f_s of 30 kH_z.

The following calculations are used to select the appropriate inductors for L_1 and L_2. For an approximate efficiency (η) of 95%, following equation can be derived

$$I_{ac} = I_{ac\_peak} \sin(\omega t) = \frac{2 \times P_0}{\eta \times V_{ac\_peak}} \sin(\omega t) \tag{8}$$

$$I_{ac\_peak} = 140 mA$$

Input current ripple is

$$\Delta I_L = 20\% I_{ac\_peak} = 28 mA$$
$$\Delta I_L = \frac{V_s \times d}{L_1 \times f_s} \tag{9}$$

The output current in a switching period is equal to the average of the fast diode current. The output average current switching period is obtained by

$$i_{dc\_avg} = 0.5 i_{dc\_peak} \Delta_1 \tag{10}$$

where, i_{dc_avg} is the peak current of fast diode and Δ_1 is the duty ratio of D, $\Delta_1 \langle 1 - d$, and i_{dc_avg} can be calculated as:

$$i_{dc\_peak} = i_{L1} + i_{L2} = \left(\frac{1}{L_{1,3}} + \frac{1}{L_2} \right) V_{ac} dT_s \tag{11}$$

$$i_{dc\_avg} = 0.5 \left(\frac{V_{ac}^2}{\left(\frac{1}{L_{1,3}} + \frac{1}{L_2} \right) V_{dc}} d^2 T_s \right) \tag{12}$$

$$I_{dc\_avg} = (1/\pi) \int_0^\pi i_{dc\_avg} d\omega t = \frac{V_{ac\_peak}^2}{4 L_e V_{dc}} d^2 T_s \tag{13}$$

where, $L_e = \frac{L_{1,3} \times L_2}{L_{1,3} + L_2}$.

From (7), the duty cycle d is calculated as:

$$d \langle \frac{V_{dc}}{V_{ac} + V_{dc}} = 0.22 \tag{14}$$

selecting $d = 0.2$, we would get

$$L_e = \frac{V_{ac\_peak}^2 \times d^2}{4 \times V_{dc} \times f_s \times I_{dc\_avg}} = 180 \mu H \tag{15}$$

L_1 and L_3 can be obtained as

$$L_{1,3} = \frac{V_{ac\_peak} \times d}{f_s \times \Delta I_L} = 8.8mH$$

$$L_1 = L_3 = L_{1,3} / 2 = 4.4mH \qquad (16)$$

Therefore, L_2 can be obtained from the following equation

$$\frac{1}{L_2} = \frac{1}{L_e} - \frac{1}{L_{1,3}} \Rightarrow L_2 = 100\mu H \qquad (17)$$

The output capacitance needed to achieve desired current ripple can be calculated as

$$C_0 = \frac{P_{load}}{V_{dc} \times \Delta V_{dc}(\%) \times 4 \times f_{ac}} = 2.2mF \qquad (18)$$

The multi loop control is proposed for the converter, outer voltage controller generating the reference current to regulate the DC voltage and the inner PI controller generating the gating signals as shown in Figure 4. The high frequency switching of the converter produces switching ripples on the DC voltage. Thus the measured DC voltage is processed through a band stop filter to eliminate the noise on the measurements.
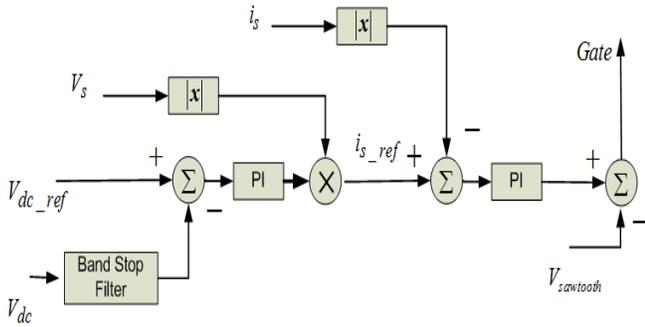

Fig. 4.   Block diagram of controller

V.   SIMULATION RESULTS

The proposed single phase bridgeless SEPIC topology is simulated by PSIM with the parameters based on the design provided in Section 4. Figure 5 presents the transient input voltage, input current, output voltage, output current and output power for the conventional bridgeless SEPIC PFC converter. Figure 6 presents the input voltage and input current for the conventional bridgeless SEPIC PFC converter.

Figure 7 presents the transient input voltage, input current, output voltage, output current and output power for the proposed bridgeless SEPIC PFC converter. Figure 8 presents the input voltage and input current for the proposed bridgeless SEPIC PFC converter. It can be seen from the Figure 8 that input current is in phase with input voltage and is sinusoidal with low THD and high PF values. Output voltage is obtained at about 10V, with a 120 Hz low frequency ripple.
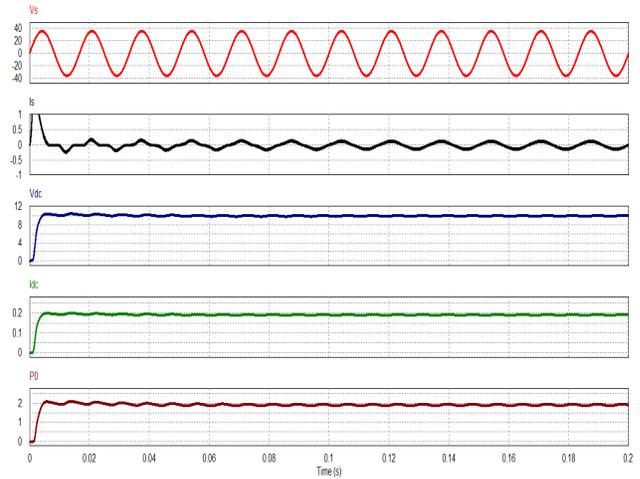

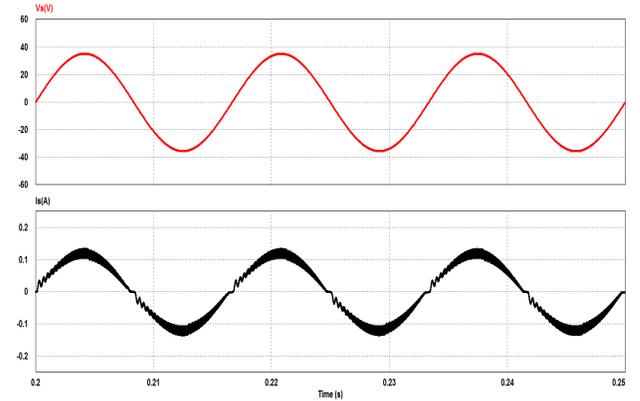Fig. 5.   The transient signals for conventional SEPIC PFC

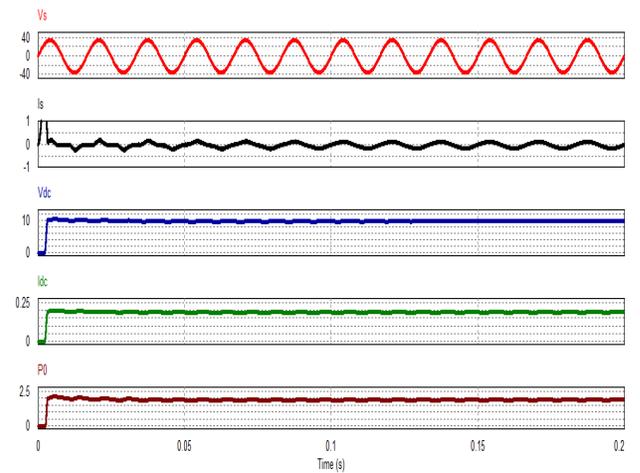Fig. 6.   The input voltage and current for conventional SEPIC PFC

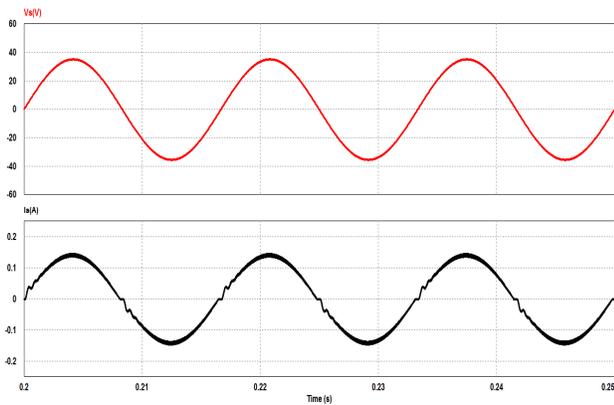Fig. 7.   The transient signals for proposed SEPIC PFC

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Fig. 8. The input voltage and current for proposed SEPIC PFC

The simulation results of the PF and THD values for a conventional SEPIC PFC converter, proposed bridgeless SEPIC PFC converter are provided in Table 1. The proposed converter is able to reduce the THD 3.23% from 8.93% and improve the power factor to 0.998. The proposed topology provides much better THD and PF compared to conventional one.

TABLE I. COMPARISON OF BRIDGELESS SEPIC PFCs

	THD (%)	PF
Conventional SEPIC PFC	8.93 %	99.3%
Proposed bridgeless SEPIC PFC	3.23%	99.8%

VI. EXPERIMENTAL RESULTS

The experimental circuit of the proposed converter is developed for the design provided in Section 4. The experimental setup is provided in Figure 9.
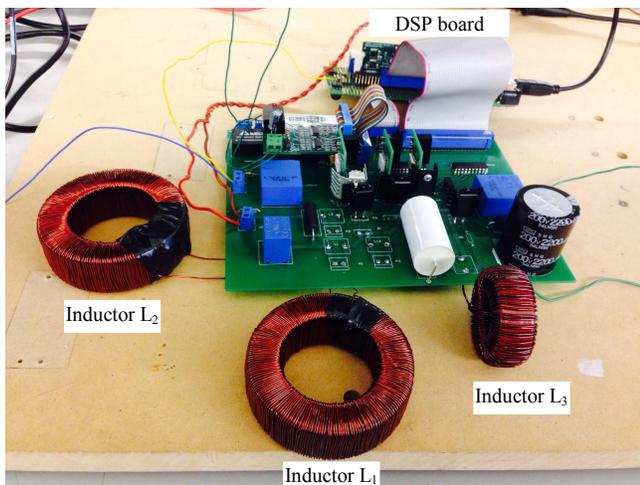

Fig. 9. The experimental prototype for proposed SEPIC converter

Input inductors L_1, L_3 and output inductor L_2 are made with toroidal core from Micro metals T300-60D (turn=205, wire= 23AWG) and T184-2 (turn=65, wire = 18AWG) respectively. IRF840PBF (500V, 8A) for switches and LXA06T600 (fast recovery, 600V, 6A, V_f=2.94V) for diodes are selected. The control circuit is implemented using a TMS320F28335 digital signal processing DSP.

The experimental results of input voltage, input current and output voltage for conventional SEPIC PFC are shown in Fig. 10 and 11. For the input voltage of 25 V_{rms}, output voltage of 10 V_{rms}, and the input current of 140 mA, the THD is measured to be 5.722%, with a power factor of 0.995

The experimental results of input voltage, input current and output voltage for the proposed SEPIC PFC are shown in Fig. 12 and13. For the input voltage of 25 V_{rms}, output voltage of 10 V_{rms}, and the input current of 136 mA, the THD is measured to be 2.837%, with a power factor of 0.998. The output voltage ripple is obtained 0.15 V at 10 Vdc as it is shown in Fig. 13. The phase of the input current is similar to the input voltage and the obtained PF is near unity.
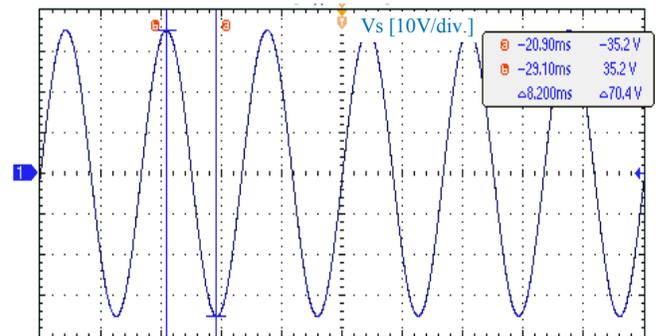
(a)
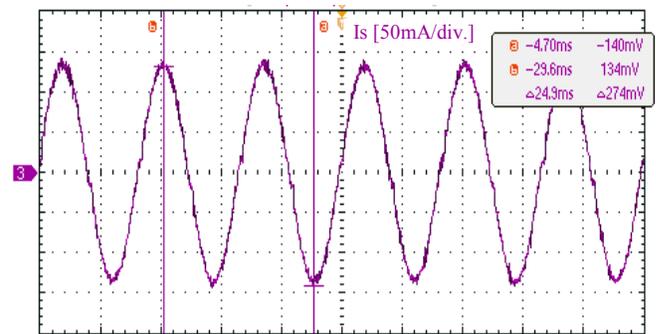
(b)

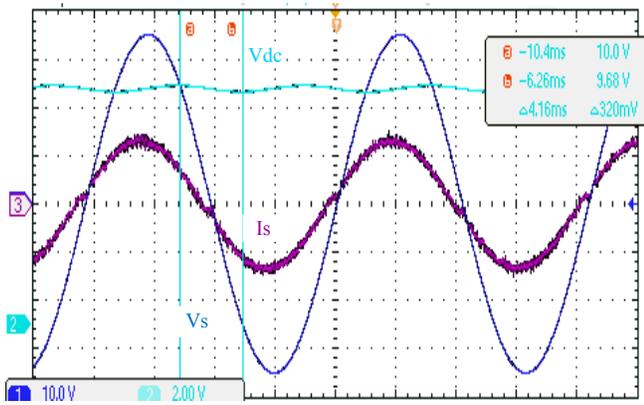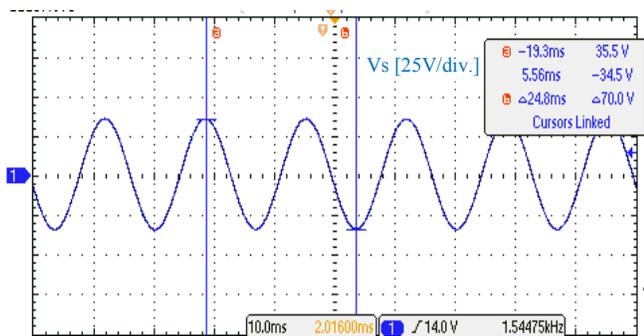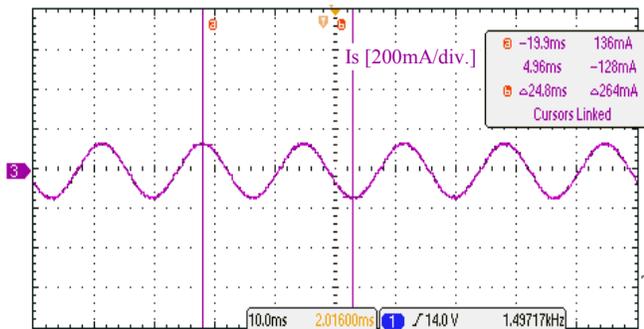Fig. 10. Experimental result for conventional SEPIC PFC. a)Input voltage and b) input current.

Fig. 11. Experimental result for conventional SEPIC PFC. *Vs*= 25 Vrms, Is = 140 mA with THD=5.722%, Vdc= 10 Vrms and PF=0.995

(a)

(b)

Fig. 12. Experimental result for proposed SEPIC PFC. a)Input voltage and b) input current.

VII. CONCLUSION

In this paper, a new single phase bridgeless SEPIC PFC converter topology is proposed, analyzed and verified with the simulations. In order to improve the power factor as well as the THD of the utility grid, the full bridge diode in input is removed. Through simulation and experimental studies the performance of the proposed SEPIC converter topology are compared with the conventional SEPIC converter topology. The proposed converter is able to reduce the THD 2.83% from 5.72% and improve the power factor to 0.998. It is found that the proposed bridgeless SEPIC PFC converter topology provides much better performance than conventional SEPIC PFC converter. The topology is implemented on a converter operating from 25 V AC input to generate 10 V DC. The proposed converter topology is proved to be very good option for single phase bridgeless SEPIC PFC solution for lower power equipments especially those requiring high quality input power.
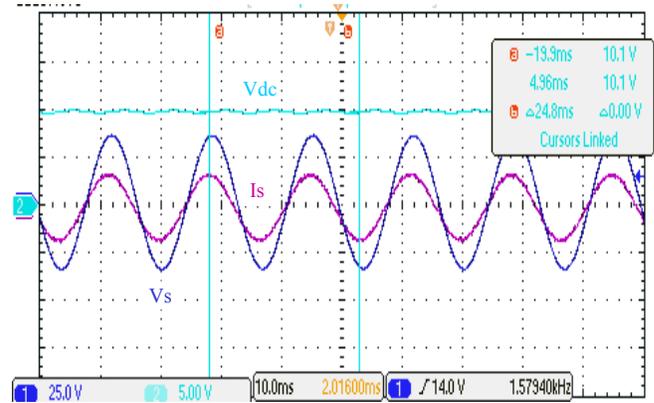

Fig. 13.   Experimental result for proposed SEPIC PFC. *Vs*= 25 Vrms, Is = 136 mA with THD=2.837, *Vdc*= 10 Vrms and PF=0.998.

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