VLSI Projects-M-Tech Projects-

S NO	TITLE
1	Low Latency and Low Error Floating-Point Sine/Cosine Function Based TCORDIC Algorithm
2	Comparative study of 16-order FIR filter design using different multiplication techniques
3	RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processin
4	RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder
5	Probabilistic Error Analysis of Approximate Recursive Multipliers
6	Optimal Design of Reversible Parity Preserving New Full Adder / Full Subtractor
7	On the Implementation of Computation-in-Memory Parallel Adder
8	Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction
9	High-Speed and Low-Power VLSI-Architecture for Inexact Speculative Adder
10	High Performance Parallel Decimal Multipliers using Hybrid BCD Codes
11	Energy-Efficient Approximate Multiplier Design using Bit Significance-Driven Logic Compression
12	Design and Analysis of Multiplier Using Approximate 15-4 Compresso
13	Sign-Magnitude Encoding for Efficient VLSI Realization of Decimal Multiplication
14	Majority-Logic-Optimized Parallel Prefix Carry Look-Ahead Adder Families Using Adiabatic Quantum-Flux-Parametron Logic
15	Energy-Efficient VLSI Realization of Binary64 Division With Redundant Number Systems
16	DSP48E Efficient Floating Point Multiplier Architectures on FPGA
17	Fast Energy Efficient Radix-16 Sequential Multiplier
18	A Residue-to-Binary Converter for the Extended Four-Moduli Set {2nâˆ’ 1, 2 n+ 1, 2 2n+ 1, 2 2n+p }
19	Majority Logic Formulations for Parallel Adder Designs at Reduced Delay and Circuit Complexity
20	Design And Synthesis Of Combinational Circuits Using Reversible Decoder In Xilinx

21	**Design of Approximate Radix-4 Booth Multipliers for Error-Tolerant Computing**
22	**Design of Power and Area Efficient Approximate Multipliers**
23	**Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers**
24	**A Slack-based Approach to Efficiently Deploy Radix 8 Booth Multipliers**
25	**A Low Error Energy-Efficient Fixed-Width Booth Multiplier with Sign-Digit-Based Conditional Probability Estimation**
26	**Design of high speed multiplier using Modified Booth Algorithm with hybrid carry look-ahead adder**
27	**An Improved Design of a Reversible Fault Tolerant LUT-Based FPGA**
28	**Energy-Aware Scheduling of FIR Filter Structures using a Timed Automata Model**
29	**Design Of High Speed Multiplier Using Modified Booth Algorithm With Hybrid Carry Look-Ahead Adder**
30	**Design Of Low Power, High Performance 2-4 And 4-16 Mixed-Logic Line Decoders**
31	**High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels**
32	**Design of Register File using Reversible Logic**
33	**Low-Quantum Cost Circuit Constructions for Adder and Symmetric Boolean Functions**
34	**Squaring in Reversible Logic using Zero Garbage and Reduced Ancillary inputs**
35	**Improved Synthesis of Reversible Sequential Circuits**
36	**A Low-Power Robust Easily Cascaded Pentamtj-Based Combinational And Sequential Circuits**
37	**Low-Power Ask Detector For Low Modulation Indexes And Rail-To-Rail Input Range**
38	**A Low-Power Incremental Deltaâ€“Sigma Adc For Cmos Image Sensors**
39	**A 55-Ghz-Bandwidth Track-And-Hold Amplifier In 28-Nm Low-Power Cmos**
40	**A Low Power Trainable Neuromorphic Integrated Circuit That Is Tolerant To Device Mismatch**
41	**Pns-Fcr: Flexible Charge Recycling Dynamic Circuit Technique For Low-Power Microprocessors**
42	**Low-Power Variation-Tolerant Nonvolatile Lookup Table Design**
43	**Dual Use Of Power Lines For Design-For-Testabilityâ€”A Cmos Receiver Design**

44 **A 28 nm Configurable Memory (TCAM/BCAM/SRAM) Using Push-Rule 6T Bit Cell Enabling Logic-in-Memory**

45 **Arithmetic algorithms for extended precision using floating-point expansions**

46 **Hybrid Lut/Multiplexer Fpga Logic Architectures**

47 **Hardware And Energy-Efficient Stochastic Lu Decomposition Scheme For Mimo Receivers**

48 **Input-Based Dynamic Reconfiguration Of Approximate Arithmetic Units For Video Encoding**

49 **High-Speedand Energy-Efficient Carry Skip Adder Operating Under A Wide Rangeof Supply Voltage Levels**

50 **VLSI Design for Convolutive Blind Source Separation**

51 **A High-Speed FPGA Implementation of an RSD-Based ECC Processor**

52 **Low-Cost High-Performance Vlsi Architecture For Montgomery Modular Multiplication**

53 **High Speed Hybrid Double Multiplication Architectures Using New Serial-Out Bit- Level Mastrovito Multipliers**

54 **A Normal I/O Order Radix-2 Fft Architecture To Process Twin Data Streams For Mimo**

55 **A Cellular Network Architecture With Polynomial Weight Functions**

56 **A Modified Partial Product Generator For Redundant Binary Multipliers**

57 **A High Throughput List Decoder Architecture for Polar Codes**

58 **A Novel Coding Scheme For Secure Communications In Distributed Rfid Systems**

59 **Design for Testability of Sleep Convention Logic**

60 **Memory-Reduced Turbo Decoding Architecture Using Nii Metric Compression**

61 **An Efficient Single and Double-Adjacent Error Correcting Parallel Decoder for the (24,12) Extended Golay Code**

62 **Low-Power Parallel Chien Search Architecture Using A Two-Step Approach**

63 **Fault Tolerant Parallel Ffts Using Error Correction Codes And Parseval Checks**

64 **Concept, Design, And Implementation Of Reconfigurable Cordic**

65 **On Efficient Retiming Of Fixed-Point Circuits**

66 **A Method to Design Single Error Correction Codes With Fast Decoding for a Subset of Critical Bits**

67 **A High-Performance Fir Filter Architecture For Fixed And Reconfigurable Applications**

68 **Flexible Dsp Accelerator Architecture Exploiting Carry-Save Arithmetic**

69 **Floating-Point Butterfly Architecture Based on Binary Signed-Digit Representation**

70 **Pre-Encoded Multipliers Based On Non-Redundant Radix-4 Signed-Digit Encoding**

71 **A 5.8-GHz Wideband TSPC Divide-by-16/17 Dual Modulus Prescaler**

72 **A GENERALIZED ALGORITHM AND RECONFIGURABLE ARCHITECTURE FOR EFFICIENT AND SCALABLE ORTHOGONAL APPROXIMATION OF DCT**

73 **DESIGN AND IMPLEMENTATION OF AREA-OPTIMIZED AES BASED ON FPGA**

74 **RECURSIVE APPROACH TO THE DESIGN OF A PARALLEL SELF-TIMED ADDER**

75 **Energy and Area Efficient Three-Input XOR/XNORs With Systematic Cell Design Methodology**

76 **RELIABLE AND ERROR DETECTION ARCHITECTURES OF POMARANCH FOR FALSE-ALARM-SENSITIVE CRYPTOGRAPHIC APPLICATIONS**

77 **A NOVEL AREA-EFFICIENT VLSI ARCHITECTURE FOR RECURSION COMPUTATION IN LTE TURBO DECODERS**

78 **NON-BINARY ORTHOGONAL LATIN SQUARE CODES FOR A MULTILEVEL PHASE CHARGE MEMORY (PCM)**

79 **LOW-POWER PROGRAMMABLE PRPG WITH TEST COMPRESSION CAPABILITIES**

80 **LOW-POWER AND AREA-EFFICIENT SHIFT REGISTER USING PULSED LATCHES**

81 **A LOW-POWER HYBRID RO PUF WITH IMPROVED THERMAL STABILITY FOR LIGHT WEIGHT APPLICATIONS**

82 **Area-Efficient Fixed-Width Squarer with Dynamic Error-Compensation Circuit**

83 **A 28 nm Configurable Memory (TCAM/BCAM/SRAM) Using Push-Rule 6T Bit Cell Enabling Logic-in-Memory**